

SERVICE MANUAL FOR

8060B



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1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the system hardware engineer specification for 8060B portable notebook computer system. The 8060B notebook computer is a new mainstream high performance thin and light notebook in the MiTAC notebook family.

1.1.2 System Overview

CPU	- Mobile Intel Banias, 1.3-1.7GHz or above - 1MB L2 Cache
Core logic	- Intel 855PM (Odem) + Intel 82801DMB (ICH4-M)
System BIOS	- Insyde 512KB Flash EPROM - Include System BIOS, VGA BIOS
Memory	- 0MB Memory onboard ; Expandable to 1.0GB - 200-pin DDR Memory Slot x2, DDR-200/266 specifications (USER Upgradeable)
VGA Controller	- nVidia NV34M; Support AGP4X - Discrete 64MB DDR VRAM (reserve for 128MB)
IDE	- Support 2 IDE channel, Up to Ultra DMA 100
LCD Display	- 15.2" TFT display; 15:10 wide screen, Resolution 1280 x 854 WXGA+
Keyboard	- Internal Key Matrix Keyboard
Touch Pad	- Intelligence Glide pad with 2 buttons.

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Audio	- Built-in AC97 V2.2 Codec - Sound Blaster Pro compatible - 3D stereo enhancement - Built-in mono microphone - Built-in 22W / 3ohm stereo speakers
Audio DJ	- 4 player buttons: Play/Pause, Next Track, Previous Track, Stop/Eject (support System Power-off play) - 1 push button and 1 LED for Audio DJ function On/Off (Push 1 second for turn-on, toggle for turn-off) - Automatically turn-off for CD player idle more than 5 minutes - Digital volume Up/Down control
PCMCIA	- Type II x1 or Type I x1; CardBus support - Non support Zoom Video/Audio Function
I/O Ports	- Bi-directional Parallel port (EPP/ECP) x 1 - USB (support USB 1.1 and USB 2.0) port x 3 - RJ-11 port x 1 - RJ-45 port x 1 - DC input x 1 - Battery Connector x1 - VGA monitor port x 1 - Line-out (SPDIF) x 1 - Mic-in x 1 - Line-in - IEEE1394 x 1 - FIR/SIR x 1 - TV-Out x 1 (7Pin S-Video connector NTSC/PAL)
MiniPCI	- 802.11b wireless LAN (optional) with built-in Antenna
LAN/MDC	- 10/100 Base-T LAN - MDC 56K, V.90 Modem
Suspend Mode	- POS (S1), Suspend to RAM (S3), Suspend to Disk (S4), Non support Wake Up on time
LED Indicator	- HDD, CD-ROM, NUM, CAP, SCROLL, Wireless LAN, Audio DJ PWR

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1. .2 System Architecture

1.2.2 Function Description

1.2.2.1 CPU

- ✦ Mobile Intel Banias processor with 400MT/s BPSB (100MHz)
- ✦ Capable of 478-pin, Micro-FCPGA processor package
- ✦ On-die 32KB instruction cache and 32KB write-back data cache
- ✦ On-die 1MB L2 cache
- ✦ Assisted Gunning Transceiver Logic (AGTL+) bus driver technology

1.2.2.2 Core Logic

- ✦ Intel 82855PM Memory Control Hub
 - Support AGP2.0 (4X AGP)
 - Support 200 and 266 MHz DDR devices
 - Maximum of 1GB of system memory by using 512MB technology devices
 - Hub Interface to ICH4-M
- ✦ Intel ICH4-M I/O Controller Hub
 - PCI 2.2 Interface
 - Bus Master IDE controller supports Ultra ATA 100/66/33

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- AC'97 2.2 Interface
- USB 1.1 and USB 2.0 Host Controllers

1.2.2.3 Memory

- ✦ Support 200/266MHZ SO-DIMMs DDR Memory expandable to 1024MB (2 SO-DIMM DDR slot).

Slot1	Slot2	Total
64MB	0	64MB
64MB	64MB	128MB
64MB	128MB	192MB
64MB	256MB	320MB
64MB	512MB	576MB
128MB	0	128MB
128MB	128MB	256MB
128MB	256MB	384MB
128MB	512MB	640MB
256MB	0	256MB
256MB	256MB	512MB
256MB	512MB	768MB
512MB	0	512MB
512MB	512MB	1024MB

Table 1. Memory Expansion Capacity

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1.2.2.4 I/O Ports

+ CRT Port

- Standard VGA compatible port
- DDC1 and DDC2B compliant

Pin	Signal	Description
1	RED	Red analog video output
2	GREEN	Green analog video output
3	BLUE	Blue analog video output
4	Monitor Sense	Monitor Sense
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	VCC	+5VDC
10	GND	Ground
11	Monitor Sense	Monitor Sense
12	CRT DATA	Data from DDC monitor
13	HSYNC	Horizontal Sync control
14	VSNC	Vertical Sync control
15	CRT CLK	Clock to DDC monitor

Table 2. CRT Connector

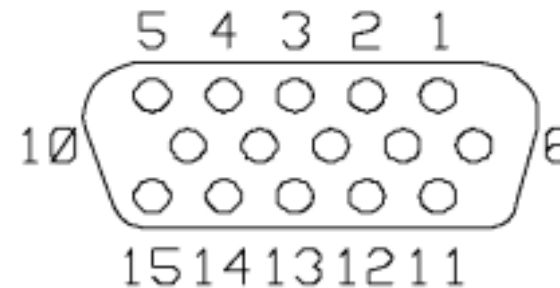


Figure 1. CRT Connector

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✚ 7 Pins S-Video port for TV-Out

- Support up 1024*768 resolution
- Support PAL and NTSC system
- Support Composite Output by a transfer cable

Pin	Signal Name	Description
1	GND	-
2	NC	-
3	COMP	O
4	GND	-
5	CRMA	O
6	NC	-
7	LUMA	O

Table 3. S-Video Port

System	Input(Active) Resolution	Active TV Lines	Over/Under Scan
NTSC	320 x 320	480 ~ 400	+
NTSC	640 x 480	480 ~ 400	+
NTSC	720 x 480	480 ~ 400	+
NTSC	720 x 400	480 ~ 400	+
NTSC	800 x 600	480 ~ 420	+
NTSC	1024 x 768	480	Over
System	Input(Active) Resolution	Active TV Lines	Over/Under Scan
PAL	320 x 320	540 ~ 500	+
PAL	640 x 480	540 ~ 500	+
PAL	720 x 480	540 ~ 500	+
PAL	720 x 400	576 ~ 510	+
PAL	800 x 600	600 ~ 510	+
PAL	1024 x 768	520	Under

Table 4. TV Out Support Modes

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✦ IEEE 1394 Port

- Supports serial bus data rates of 100, 200, and 400Mbps/second
- The Asynchronous and Isochronous data transfers are supported
- One IEEE1394 port supported

Pin	Signal Name	Description
1	TPB-	I/O
2	TPB+	I/O
3	TPA-	I/O
4	TPA+	I/O

Table 5. IEEE1394 Port

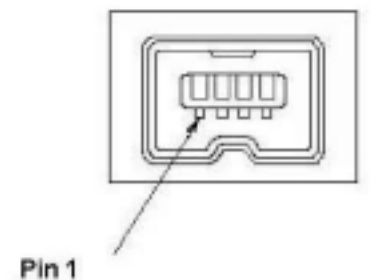


Figure 2. 1394 Connector

✦ Audio Ports

- SPDIF
- Microphone In & Line In
- Built In 2 high quality internal speaker (1W / 8 ohm with Box)
- Built in 1 mono microphone
- AC97 V2.2 compliance.

	Internal Speaker	Internal Microphone	LED of SPDIF
Plug Ear-Phone In	Mute	Active	Off
Plug SPDIF Device In	Mute	Active	On
Plug External Microphone	Mute	Mute	Off

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✚ RJ-11

- Connection to Modem Daughter Board Connector
- Support 56Kbps/V.90

Pin	Signal Name	Direction	Description
1	NC	-	No Connect
2	LINE +	I/O	Phone Line Positive
3	LINE -	I/O	Phone Line Negative
4	NC	-	No Connect

Table 6. Modem Port

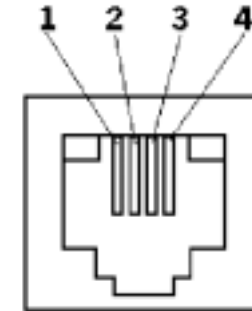


Figure 3. Modem Connector

✚ RJ-45

- Support full duplex 10 Base-T, 100 Base-T Ethernet

Pin	Signal Name	Direction	Description
1	TX +	OUT	Transmit Data Ring
2	TX -	OUT	Transmit Data Tip
3	RX +	IN	Receive Data Ring
4	TERM 1	-	Internal termination resistor
5	TERM 2	-	Internal termination resistor
6	RX	IN	Receive Data Tip
7	TERM 3	-	Internal termination resistor
8	TERM 4	-	Internal termination resistor

Table 7. LAN Port

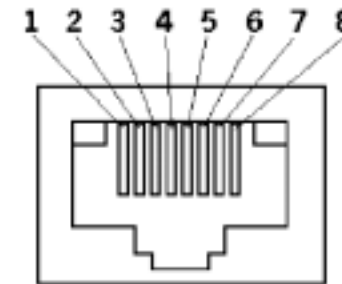


Figure 4. LAN Connector

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✦ Infrared interface supporting IRDA format

- FIR IrDA 1.1 compliant.
- HP-SIR supported.

✦ USB Ports

- Three industry standard USB 2.0 ports
- Support MAX. Power Current 500mA each port

Pin	Signal Name	Direction	Description
1	VCC	-	USB Device Power (+5VDC)
2	DATA-	I/O	Balanced Data Negative
3	DATA+	I/O	Balanced Data Positive
4	GND	-	Ground

Table 8. USB Port

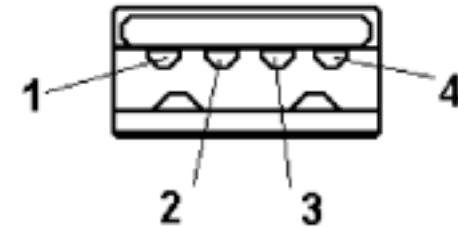


Figure 5. USB Connector

✦ Parallel Port

- Configurable as logical ports LPT1 , LPT2 or LPT3
- EPP rev 1.7 & 1.9 compatible
- ECP (IEEE 1284) compatible
- Industry standard 25 Pins connector

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Pin	Signal Name	Direction	Description
1	STROBE#	O	Data Strobe
2	PD0	I/O	PP Data bit 0
3	PD1	I/O	PP Data bit 1
4	PD2	I/O	PP Data bit 2
5	PD3	I/O	PP Data bit 3
6	PD4	I/O	PP Data bit 4
7	PD5	I/O	PP Data bit 5
8	PD6	I/O	PP Data bit 6
9	PD7	I/O	PP Data bit 7
10	-ACK	I	Printer Acknowledge
11	BUSY	I	Printer Busy
12	PE	I	Paper Out
13	SLCT	I	Print Select Acknowledge
14	-AUTOFDXT	O	Auto Line Feed
15	-ERROR	I	Printer Error
16	-INIT	O	Reset Printer
17	SLCTIN#	I	Ground
18	GND	-	Ground
19	GND	-	Ground
20	GND	-	Ground
21	GND	-	Ground
22	GND	-	Ground
23	GND	-	Ground
24	GND	-	Ground
25	GND	-	Ground
Case		-	Ground

Table 9. Parallel Port

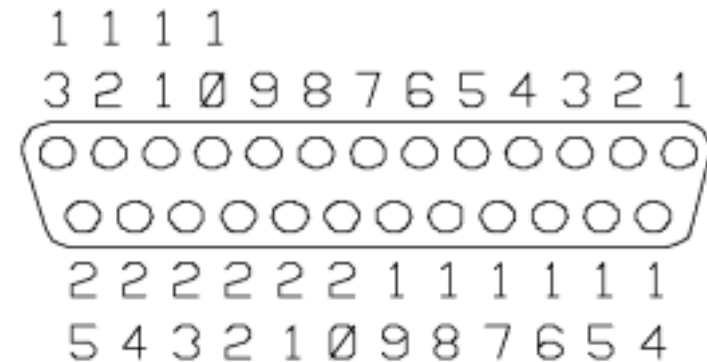


Figure 6. Parallel Port Connector

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1.2.2.5 PC Card Slot

- ✦ One Type II/I slot supporting the 1997 PC Card standard, and including full R2 (16-bit) and 32-bit Cardbus data transfer
- ✦ TI PCI4510 (PCMCIA Controller) & TI TPS2211A (Power Switch)

1.2.2.6 Graphical Subsystem

- ✦ nVIDIA NV34M graphical controller
- ✦ AGP4X including power management pins
- ✦ 256-bit 3D and 2D graphics accelerator
- ✦ Dual channel LVDS
- ✦ TV-out support for NTSC and PAL
- ✦ Microsoft DirectX and OpenGL Optimizations and support

1.2.2.7 Display

- ✦ 15.2" TFT display; 15:10 wide screen, Resolution 1280x854 WXGA+
- ✦ External Video refresh rate of up to 100Hz supported
 - Vertical refresh frequencies to meet VESA requirements
 - Simultaneous video in specified video modes – switchable with hot key

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1.2.2.8 IDE Interface

- ✦ Support Dual Independent IDE Channels, One is Hard Disk. The other one is Optical Device
- ✦ Supports PIO mode 0,1,2,3,4 and Ultra DMA 33/66/100

1.2.2.9 Read Only Memory (BIOS Flash)

- ✦ Fully compatible with industry standard software including Windows 2000 & Windows XP
- ✦ Fully supports APM V1.2 and latest ACPI specification
- ✦ 4Mb Flash BIOS
- ✦ Insyde BIOS core

1.2.2.10 Power Management Features

- ✦ Local standby mode (Individual devices such as HDD, graphics controller, LCD etc..)
- ✦ CPU Idle mode (Including ACPI modes C1 and C2)
- ✦ Suspend mode (Including S1 and S3 ACPI modes)
- ✦ Fully APM V1.2 compliant
- ✦ Fully ACPI V1.1 compliant
- ✦ Hibernate for Windows 2000 and Windows XP

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- ✦ Thermal management
- ✦ Fully US EPA Energy Star compliant

1.2.2.11 Keyboard Controller

- ✦ Hitachi H8-3437S

1.2.2.12 Super I/O

- ✦ NS PC87393F LPC interface Ultra I/O

1.2.2.13 LEDs Indicator

- ✦ HDD & CDROM & NUM & CAP & SCROLL & Wireless LAN & Audio DJ POWER

1.2.2.14 Buttons

- ✦ One Power Button
- ✦ 7 Audio Control Buttons

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1.2.2.15 Touch Pad Module

- ✦ Synaptics TM41P-350 with two Buttons

1.2.2.16 Audio DJ

- ✦ Seven Audio Control Buttons
 - PLAY_PAUSE
 - NEXT_TRK/SCAN_FW
 - PREV_TRK/SCAN_RW
 - STOP_EJECT
 - Volume up (Digital Volume Control)
 - Volume Down (Digital Volume Control)
 - Power on / off Audio DJ
- ✦ Allowing CD play while the notebook is OFF
- ✦ Low power consumption
- ✦ Automatically turn-off for CD player idle more than 5 minutes

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1.2.2.17 MODEM (MDC) - Option

Pin	Signal Name	Pin	Signal Name
1	MONO_OUT	2	NC
3	NC	4	MODEM_SPK
5	NC	6	NC
7	NC	8	GND
9	NC	10	+5V
11	NC	12	NC
13	NC	14	NC
15	GND	16	Pull Up to +3V
17	+3V	18	+5V
19	GND	20	GND
21	+3V	22	ACSYNC
23	ACSDOUT	24	MSDIN
25	-ACRST	26	MSDIN
27	GND	28	GND
29	GND	30	ACBITCLK

Table 10. Modem Daughter Board Connector

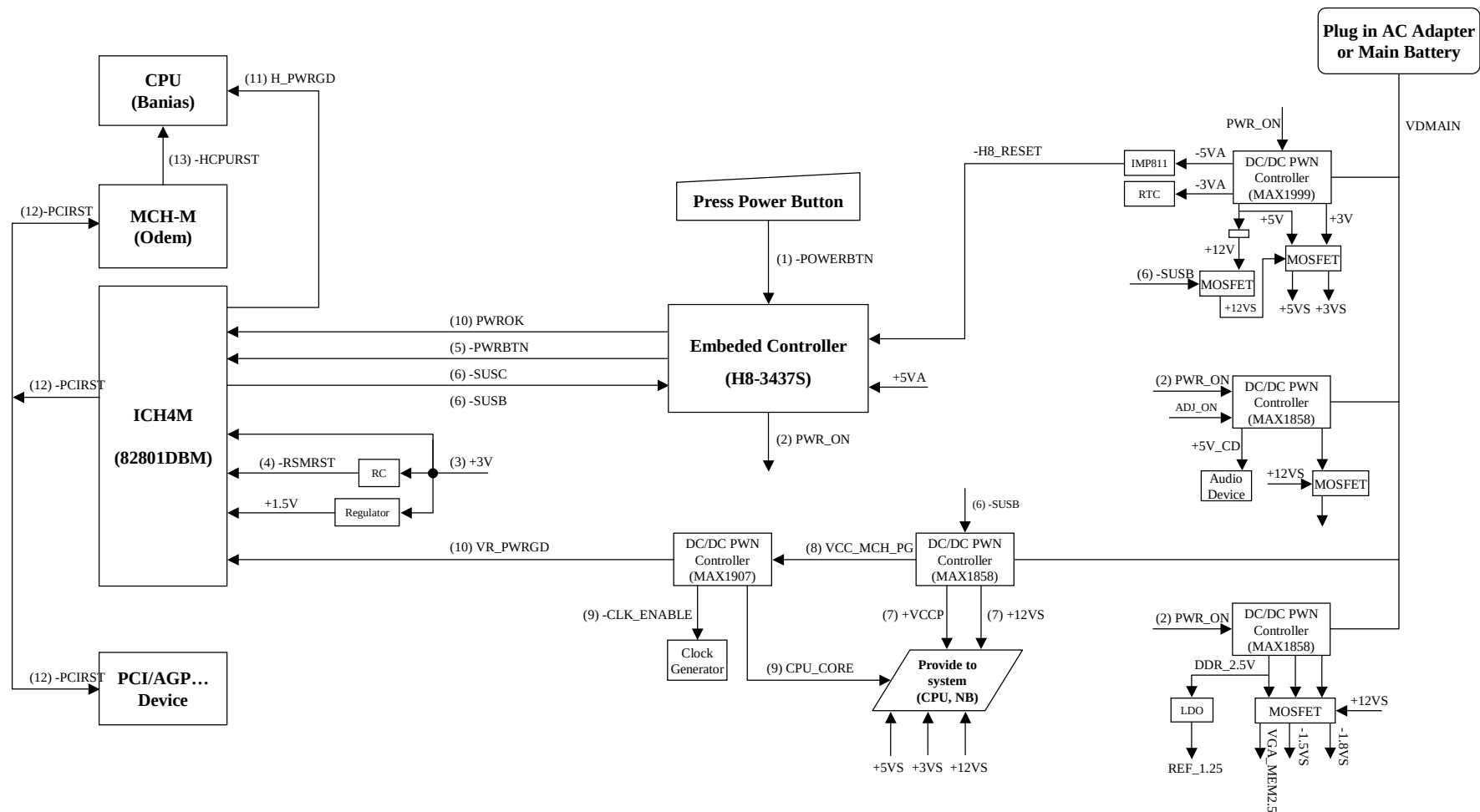
1.2.2.18 Mini PCI

- ✚ MiniPCI Specification V1.0
- ✚ 802.11b wireless LAN (optional) with built-in Antenna

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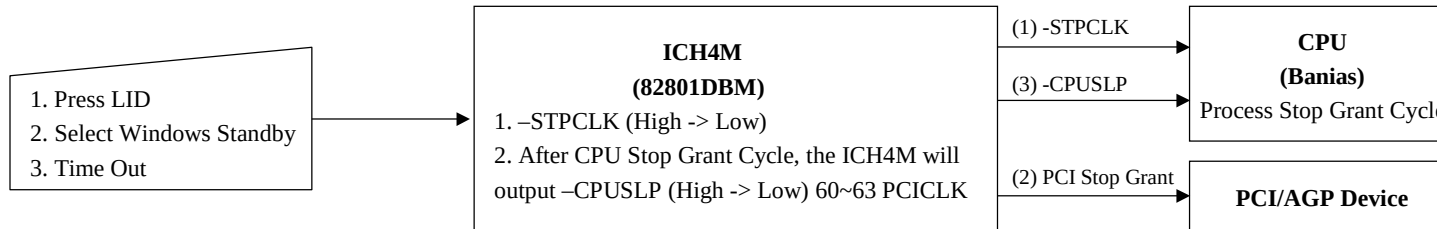
1.3 Electrical Characteristic

1.3.1 Power On Sequence

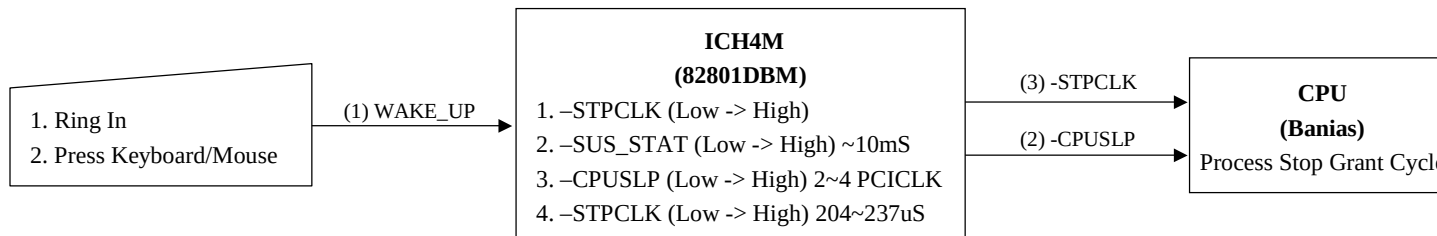


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1.3.2 Power On Suspend Sequence

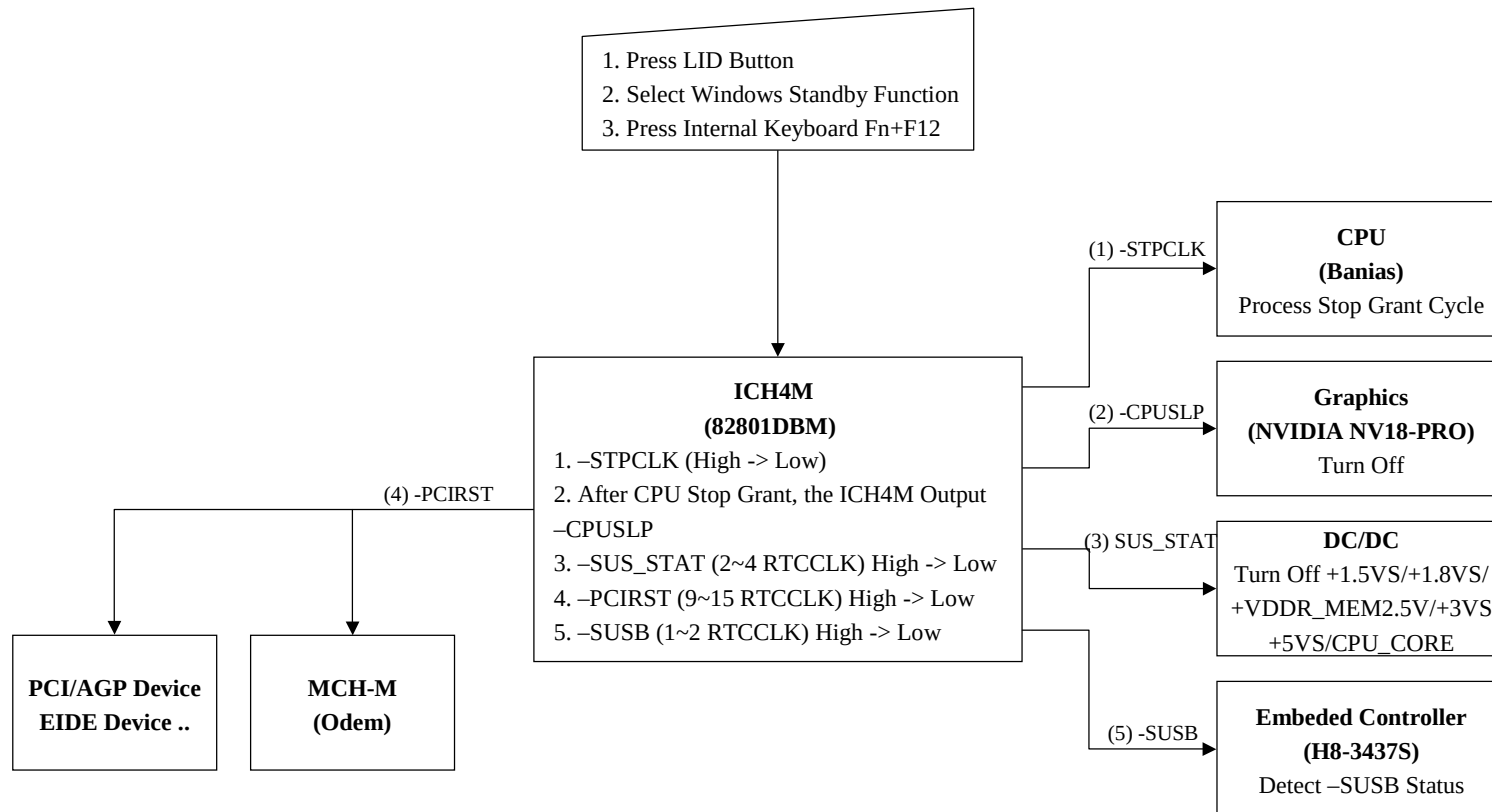


1.3.3 Resume from Power On Suspend Sequence



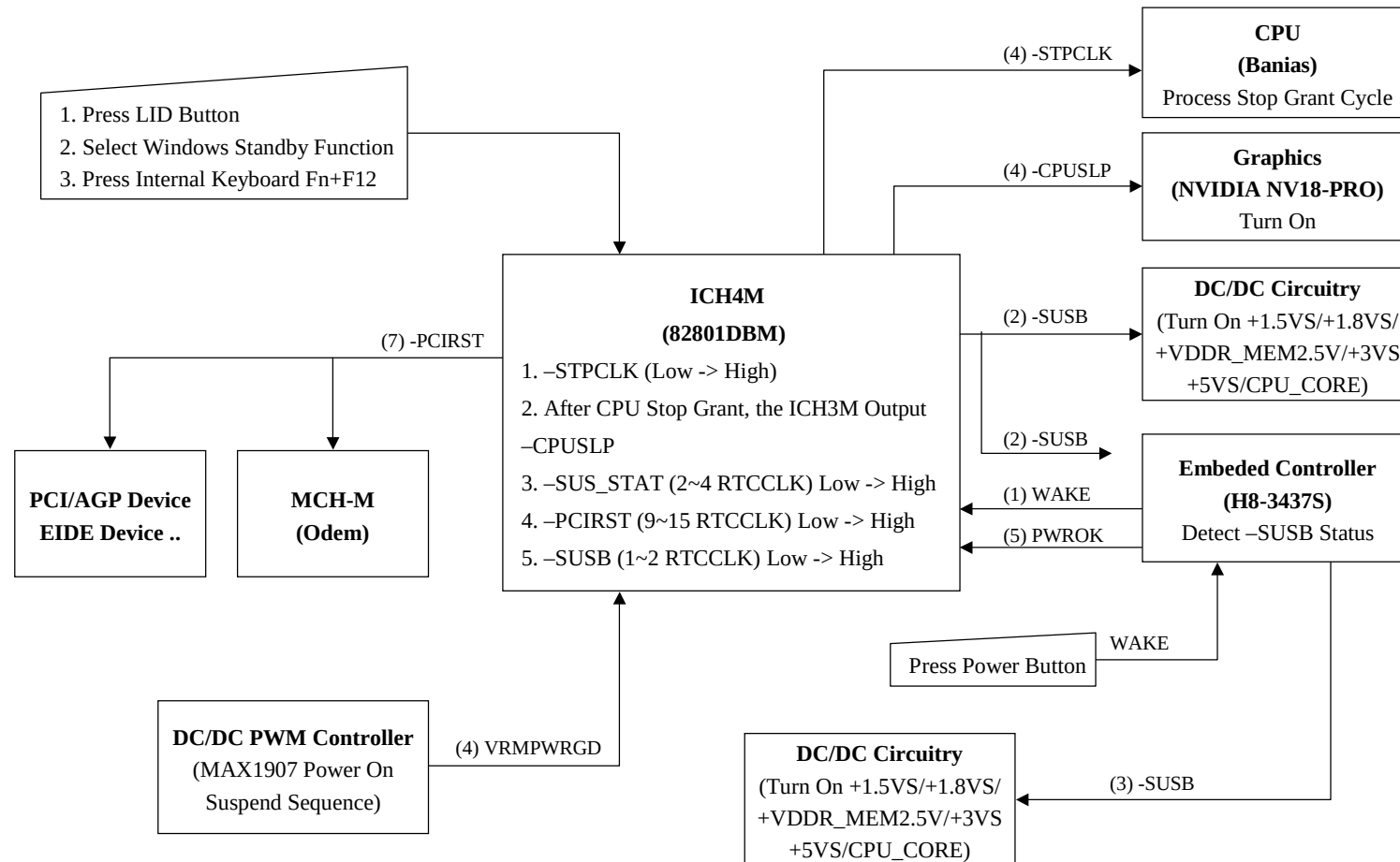
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1.3.4 Suspend To RAM Sequence



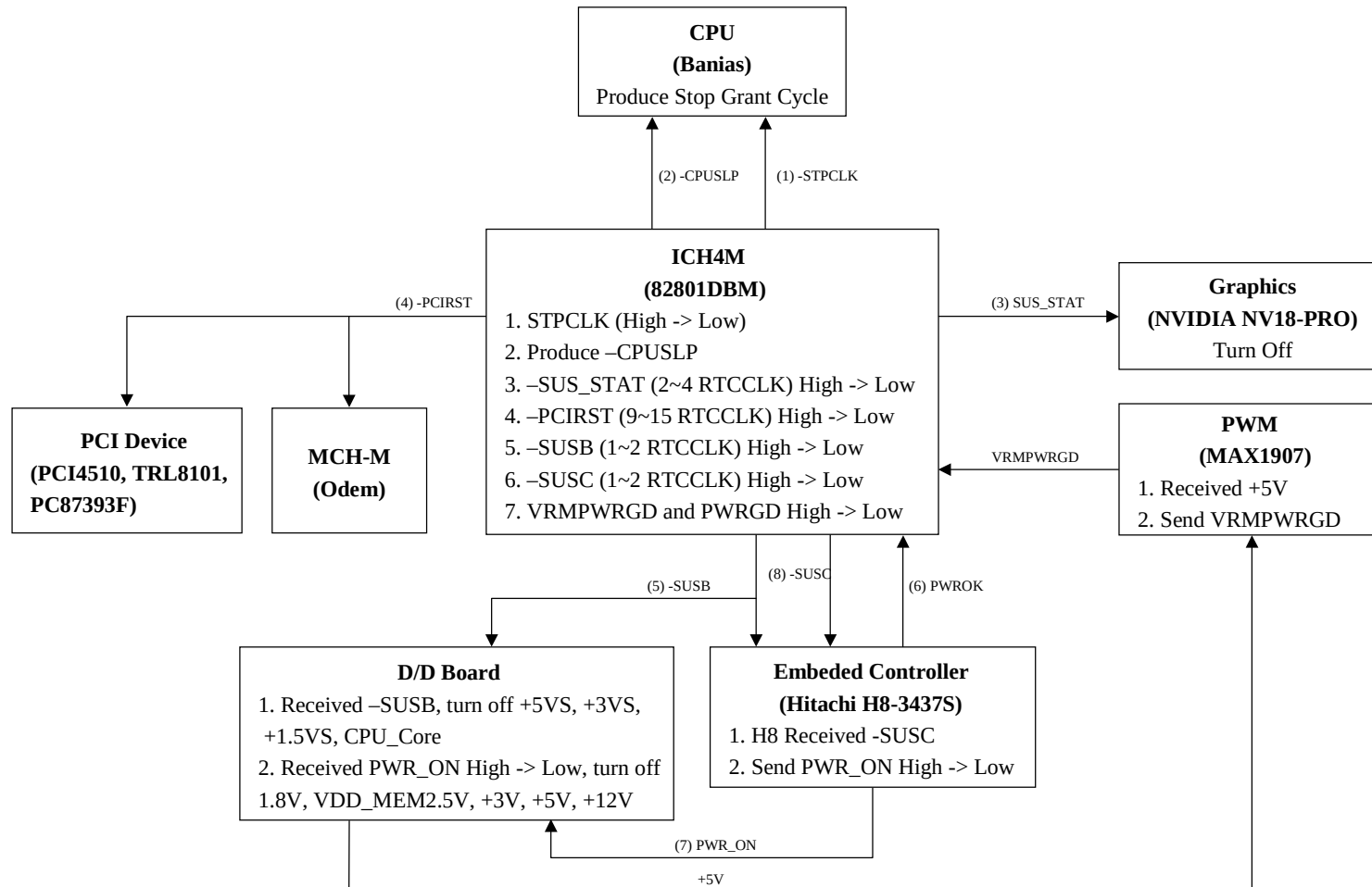
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1.3.5 Resume from Suspend To RAM Sequence



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1.3.6 Suspend to Disk Sequence



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1.3.7 ICH4-M (82801DBM) GPI/O Pin Define

Pin Name	Signal Name	Power Plane	Type Plane	Original Type	During PCIRST#	Immediately after PCIRST#	S1	S3	S4/S5	Description
GPIO0/REQA#	-PCI_REQA	+3.3VS	I	I			Driven	Low	Low	
GPIO1/REQB#/REQ5#	-PCI_REQB	+3.3VS	I	I			Driven	Low	Low	
GPIO2/PIRQE#	-PCI_INTE	+3.3VS	I	I	High - 2	High - 2	High - 2	Off	Off	
GPIO3/PIRQF#	-PCI_INTF	+3.3VS	I	I	High - 2	High - 2	High - 2	Off	Off	
GPIO4/PIRQG#	-PCI_INTG	+3.3VS	I	I	High - 2	High - 2	High - 2	Off	Off	
GPIO5/PIRQH#	-PCI_INTH	+3.3VS	I	I	High - 2	High - 2	High - 2	Off	Off	
GPIO6	-AGP_BUSY	+3.3VS	I	I			High	Low	Low	
GPIO7	TP	+3.3VS	I	I						not Implement
GPIO8	-SCI	+3.3V_ICH	I	I	High	High	High	High	Off	
GPIO9				I						not Implement
GPIO10				I						not Implement
GPIO11/SMBALERT#	-SMB_ALERT	+3.3V_ICH		I			Driven	Driven	Driven	
GPIO12	-EXTSMI	+3.3V_ICH	I	I	High	High	High	High	Off	
GPIO13	TP	+3.3V_ICH	I	I						not Implement
GPIO14				I						not Implement
GPIO15				I						not Implement
GPIO16/GNTA#	-PCI_GNTA/TP	+3.3VS	O	O	High - 2	High	High	Off	Off	not Implement
GPIO17/GNTB#/GNT5#	-PCI_GNTB/TP	+3.3VS	O	O	High - 2	High	High	Off	Off	not Implement
GPIO18				O						not Implement
GPIO19	-SUSA	+3.3VS	O	O	High	High	Low	Off	Off	
GPIO20				O						not Implement
GPIO21/C3_STAT#	-C3_STAT/TP	+3.3VS	O	O	High	High	Low	Off	Off	
GPIO22	-CPUPERF	+3.3VS	O	OD	High - 2	High - 2	High	Off	Off	

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Continued to the previous table

Pin Name	Signal Name	Power Plane	Type Plane	Original Type	During PCIRST#	Immediately after PCIRST#	S1	S3	S4/S5	Description
GPIO23	SSMUXSEL/TP	+3.3VS		O	Low	Low		Off	Off	
GPIO24	PCLKRUN	+3.3VS	I/O	I/O	Low	Low	High	Off	Off	
GPIO25	-1394PWR	+3.3V_ICH	O	I/O	High	High	High	High	Off	
GPIO26										not Implement
GPIO27	-PCIRST_MSK	+3.3V_ICH	O	I/O	High	High	High	High	Off	
GPIO28	-GATE1394	+3.3V_ICH	O	I/O	High	High	High	High	Off	
GPIO29			O	O						
GPIO30			O	O						not Implement
GPIO31				O						not Implement
GPIO32	-MPCIACT	+3.3VS	O	I/O	High	High	Low	Off	Off	
GPIO33	GPIO33	+3V	O	I/O	High	High	High	Off	Off	
GPIO34	-ENABKL_MSK	+3.3VS	O	I/O	High	High	High	Off	Off	
GPIO35	-HDD_RST	+3.3VS	O	I/O	High	High	High	Off	Off	
GPIO36	-CDROM_RST	+3.3VS	O	I/O	High	High	High	Off	Off	
GPIO37	SPK_OFF	+3.3VS	O	I/O	High	High	High	Off	Off	
GPIO38	NC	+3.3VS	O	I/O						not Implement
GPIO39	NC	+3.3VS	O	I/O						not Implement
GPIO40	NC	+3.3VS	O	I/O						not Implement
GPIO41	NC	+3.3VS	O	I/O						not Implement
GPIO42	NC	+3.3VS	O	I/O						not Implement
GPIO43	NC	+3.3VS	O	I/O						not Implement
GPIO[44:47]										not Implement

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1.3.8 Keyboard Controller Pin Define

Pin	Port	Signal Name	Type	Connect To	Description
79~72	P10~P17	KO[0:7]	O	Internal Keyboard	Keyboard Matrix
67~60	P20~P27	KO[8:15]	O	Internal Keyboard	Keyboard Matrix
82~89	P30~P37	SD[0:7]	I/O	Super I/O	ISA Data Bus
49	P40	-CONN_RW	I	OZ165	Audio DJ Scan RW
50	P41	-H8_WAKE_UP	O	ICH3M	Connect to chipset ICH3M to wake up system
51	P42	-H8_SMI	O	ICH3M	Connect to chipset ICH3M to system management interrupt (Non-ACPI mode)
52	P43	H8_SCI	O	ICH3M	Connect to chipset ICH3M to system configuration interrupt (ACPI mode)
53	P44	IRQ1	O	Super I/O	IRQ for Keyboard
54	P45	IRQ12	O	Super I/O	IRQ for Mouse
55	P46	-FAN2	O	FAN2	Control system fan on & turn on/off duty
56	P47	-FAN1	O	FAN1	Control CPU fan on & turn on/off duty
14	P50	PWR_ON	O	DC/DC Connector	Control system power on/off
13	P51	-H8_RCIN	O	ICH3M	Keyboard reset
12	P52	LEARNING	O	DD Board	Control DD board voltage, negative logic
26~29	P60~P63	KI[0:3]	I	Internal Keyboard	Keyboard Matrix
32~35	P64~P67	KI[4:7]	I	Internal Keyboard	Keyboard Matrix
1	RESET	-H8_RESET	I	MAX809	Reset H8-F3437
7	NM#	-H8_SUSB	I	ICH3M	STR indicator
8	STBY	-H8_STBY	I	Pull-Up	No use
10	PA7	T_CLK	I/O	Touch PAD	Connect to Touch Pad clock
11	PA6	-ADJ_BTN	I	OZ165	Audio DJ Power Button
20	PA5	-CONN_STOPEJECT	I	OZ165	Audio DJ CD-ROM Stop and Eject
21	PA4	H8_PWROK	O	ICH3M	System Power Ready

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Continued to the previous table

Pin	Port	Signal Name	Type	Connect To	Description
30	PA3	-ADEN	I	D/D Connector	Adaptor in
31	PA2	-CONN_PLAYPAUSE	O	OZ165	Audio DJ Play and Pause
47	PA1	-BATT_EDAD	I	Power Circuitry	Indicated the battery capacity is not enough to power on system
48	PA0	-RI	I	LAN/CARD BUS	If system on suspend mode, then received this signal & system have to wake up
57	PB7	T_DATA	I/O	Touch PAD	Connect to Touch Pad DATA
58	PB6	ADJ_ON	I	OZ165	Control OZ165 Power
68	PB5	-CONN_FF	I	OZ165	Audio DJ Scan FF
69	PB4	CHARGING	O	Charge Circuitry	Indicated charge circuitry to work
80	PB3	FAN1_SPD	I	FAN1	Return FAN1 (CPU FAN) Speed
81	PB2	FAN2_SPD	I	FAN2	Return FAN2 (System FAN) Speed
90	PB1	LED_DATA	O	74164	(Bit 0-7: -SCROLL, -NUM, -CAP, -AC POWER, -BATT POWER, BATTR, -BATT_G)
91	PB0	LED_CLK	O	74164	For LED indicated
5	MD1	H8_MODE1	I	Pull-Up	H8 Mode select
6	MD0	H8_MODE0	I	Pull-Up	H8 Mode select
16	P97	BAT_DATA	I/O	BAT_H8	SM_BUS DATA for Smart Battery
17	P96	H8_A20GATE	I	ICH3M	For A20M
18	P95	-H8_ICH3BTN	O	ICH3M	Button to ICH3M
10	P94	SW_+5VA	O	LP-2951	To switch +5V/+5VA power source
22	P93	-H8_THRM	O	ICH3M	To ICH3M, Requesting the system to enter power management mode, clock throttling
23	P92	-PWERBTN	I	Power Button	System power button
24	P91	-LID	I	LID switch	Cover switch, logic low means LCD cover closed
25	P90	-H8_SUSC	I	ICH3M	System inter S4~S5, positive logic
99	P86	BAT_CLK	I/O	Battery	SM_BUS clock for Smart Battery

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Continued to the previous table

Pin	Port	Signal Name	Type	Connect To	Description
98	P85	-H8_MCCS	I	Super I/O	Port 60h/64h chip select
97	P84	-IOW	I	Super I/O	Input/Output Write
96	P83	-IOR	I	Super I/O	Input/Output Red
95	P82	-H8_KBCS	I	Super I/O	Port 62h/66h chip select
94	P81	H8_A20GATE	O	ICH3M	For A20M
93	P80	SA2	I	Super I/O	ISA address
45	P77	BLADJ	O	Inverter	Back/Light adjust control
44	P76	CHG_I	O	Charger Circuitry	
43	P75	+5VS	I		+5VS monitor
42	P74	+5V	I		+5V monitor
41	P73	+1.8VS	I		+1.8VS monitor
40	P72	I_LIMIT	I	Charge	For battery charge
39	P71	BAT_VOLT	I	Battery	Report battery voltage
38	P70	BAT_TEMP	I	Battery	Report battery thermal

1.3.9 Power Consumption of Suspend Mode

- ✦ Suspend to RAM < 90mA
- ✦ Suspend to Disk /Soft-off /Mechanical off < TBDmA

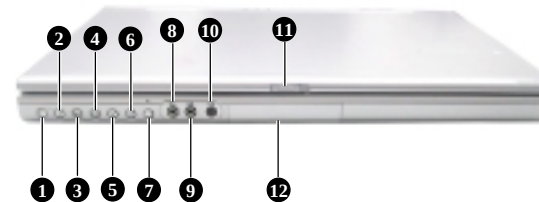
8060B N/B Maintenance

2. System View and Disassembly

2.1 System View

2.1.1 Front View

- ❶ Turn 🎵 Down Button
- ❷ Turn 🎵 Up Button
- ❸ Stop/Eject Button
- ❹ Play/Pause Button
- ❺ ▶|| Button
- ❻ ||◀ Button
- ❼ CD/DVD-ROM Power Button
- ❽ External Microphone Jack
- ❾ Line Out Phone Jack
- ❿ Line Out Phone Jack
- ⓫ Top Cover Latch
- ⓬ Hard Disk Drive



2.1.2 Left-side View

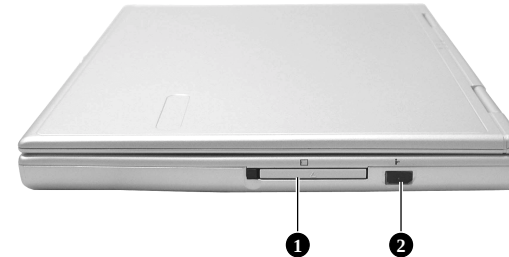
- ❶ CD/DVD Disk Drive



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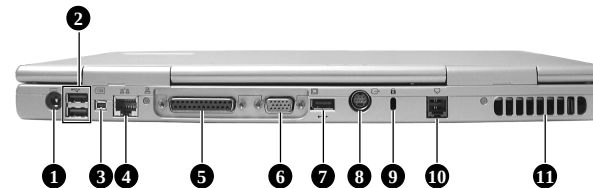
2.1.3 Right-side View

- ❶ PCMCIA Card Socket
- ❷ IR Sensor



2.1.4 Rear View

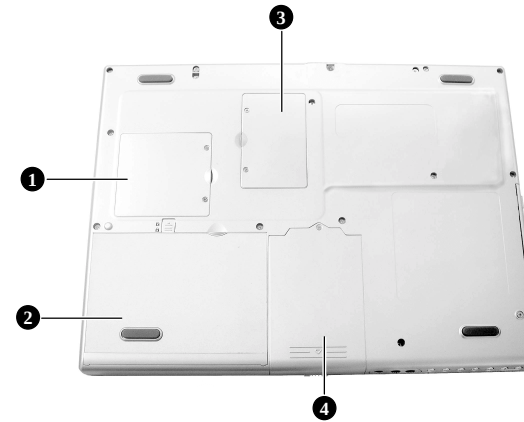
- ❶ Power Connector
- ❷ USB Ports
- ❸ 1394 Jack
- ❹ RJ-45 Connector
- ❺ Parallel Port
- ❻ VGA Port
- ❼ System Fan
- ❽ S-Video Output Connector
- ❾ Kensington Lock
- ❿ RJ-11 Connector
- ⓫ Ventilation Openings



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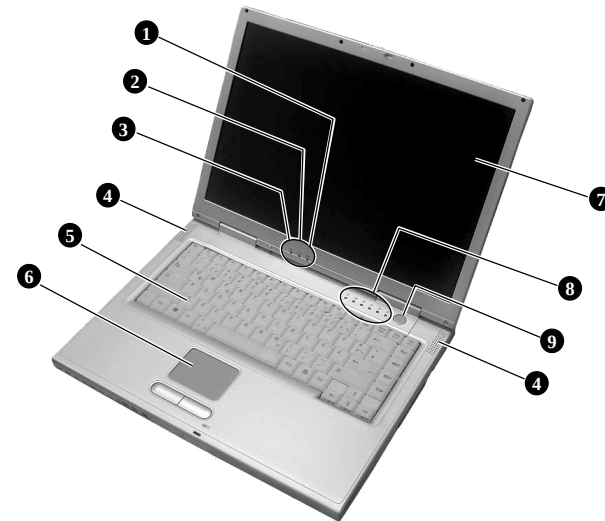
2.1.5 Bottom View

- ❶ Wireless Card
- ❷ Battery Pack
- ❸ Extend SO-DIMM
- ❹ Hard Disk Drive



2.1.6 Top-open View

- ❶ Battery Charge Indicator
- ❷ Battery Power Indicator
- ❸ AC Power Indicator
- ❹ Microphone
- ❺ Keyboard
- ❻ Touch Pad
- ❼ LCD Screen
- ❽ Device Indicators
- ❾ Power Button



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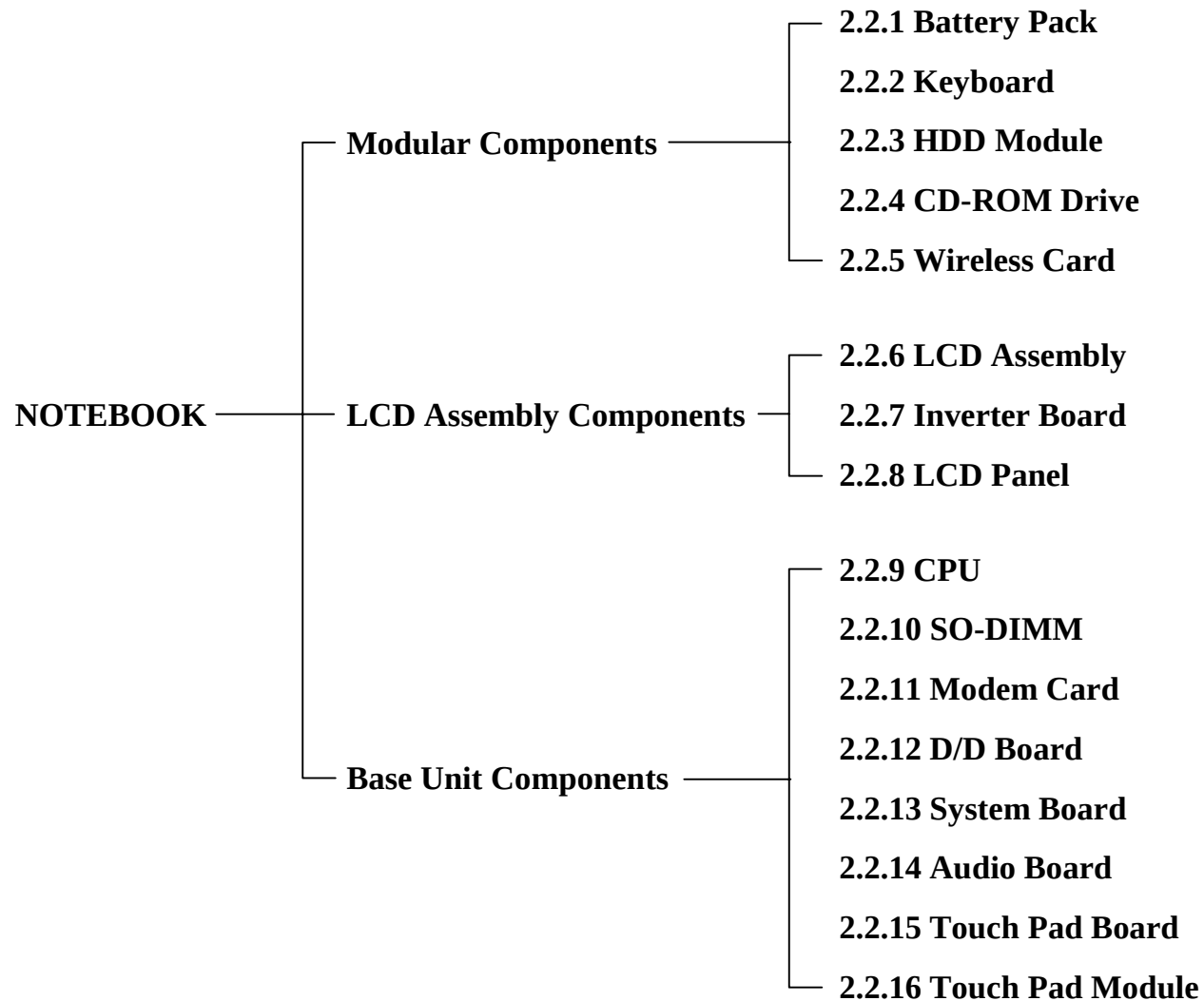
2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *1. Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*

*2. During disassembly, 1) Label each cable as you disconnect it, noting its position and routing;
2) Keep all the screws.*

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2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the release lever to the “unlock” () position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

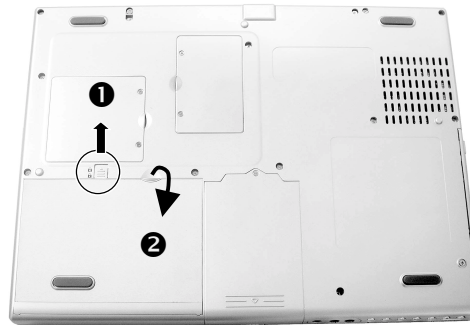


Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the “lock” () position.

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2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (See section 2.2.1 Disassembly)
2. Open the top cover.
3. Loosen the four latches locking the keyboard. (Figure 2-2)



Figure 2-2 Loosen the four latches

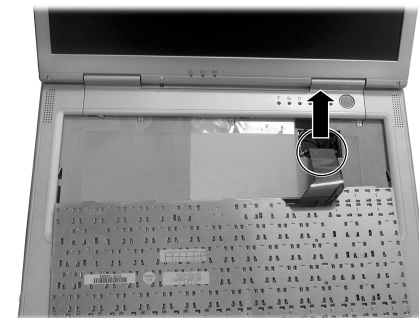


Figure 2-3 Disconnect the cable

4. Slightly lift up the keyboard and disconnect the cable from the mother board, then separate the keyboard. (Figure 2-3)

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place with four latches. .
2. Replace the battery pack. (See section 2.2.1 Reassembly)

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2.2.3 HDD Module

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove one screw and slide out the HDD compartment cover. (Figure 2-4)
4. Slide HDD module out from the compartment carefully. (Figure 2-5)



Figure 2-4 Remove HDD module

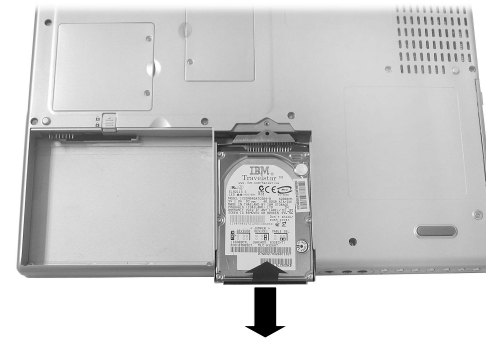


Figure 2-5 Disassemble the hard disk

Reassembly

1. Slide the HDD module into the compartment , then replace the HDD compartment cover.
2. Replace the battery pack. (See section 2.2.1 Reassembly)

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2.2.4 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.2.1 Disassembly)
2. Remove the HDD module. (See section 2.2.3 Disassembly)
3. Remove one screw fastening the CD/DVD-ROM drive. (Figure 2-6)
4. Then insert a small rod, such as a straightened paper clip, into the drive's manual eject hole and push firmly to release the tray (❶). Pull the tray out until fully extended, then carefully pull harder to remove the CD/DVD-ROM drive (❷). (Figure 2-7)

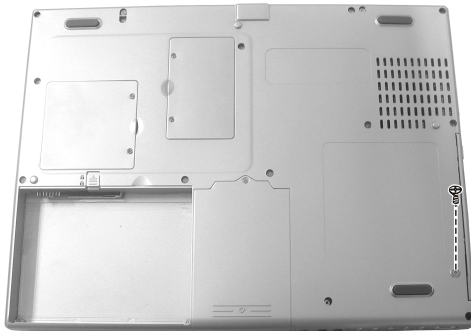


Figure 2-6 Remove one screw



Figure 2-7 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with one screw.
2. Replace the HDD module. (See section 2.2.3 Reassembly)
3. Replace the battery pack. (See section 2.2.1 Reassembly)

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2.2.5 Wireless Card

Disassembly

Complete the steps in [Section 2.2](#) to prepare the system for disassembly.

1. Remove the battery pack. (See section 2.2.1 Disassembly)
2. Remove two screws fastening the mini PCI cover. (Figure 2-8)
3. Disconnect the antenna connecting the wireless card. (Figure 2-9 step 1)

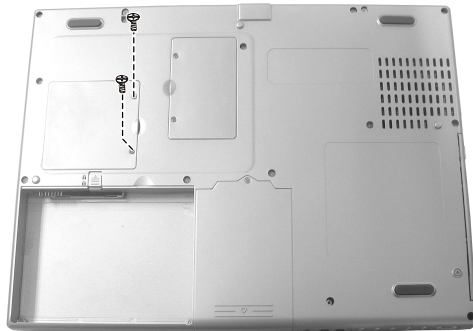


Figure 2-8 Remove the mini PCI cover

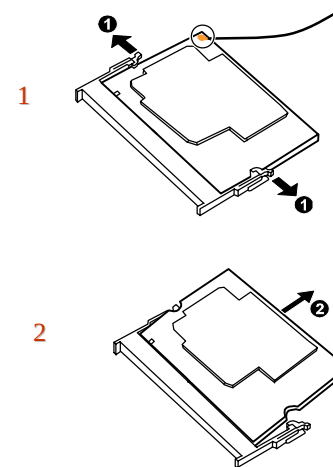


Figure 2-9 Remove the antenna

4. Pull the retaining clips outwards (❶) and remove the wireless card (❷). (Figure 2-9 step 2)

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Reassembly

1. To install the wireless card, match the wireless card's notched part with the socket's projected part and firmly insert the card into the socket. Then push down until the retaining clips lock the card into the socket.
2. Attach the antenna. Then replace the cover and secure with two screws.
3. Replace the battery pack. (See section 2.2.1 Reassembly)

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2.2.6 LCD ASSY

Disassembly

1. Remove the battery pack and keyboard. (See sections 2.2.1 and 2.2.2 Disassembly)
2. Carefully upside down the notebook, then remove two screws on the bottom of the notebook. (Figure 2-10)
3. Disconnect the antenna from the wireless card. (See the step 1, 2 of section 2.2.5 Disassembly)
4. Turnover the notebook and remove two screws on the rear side of the notebook. (Figure 2-11)

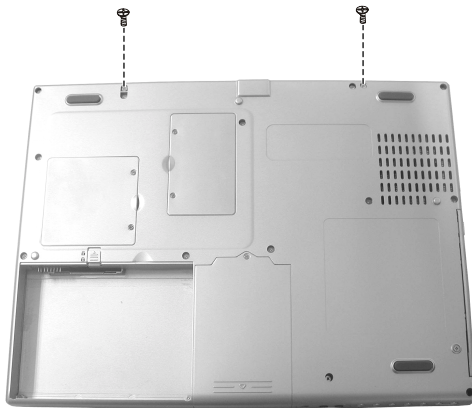


Figure 2-10 Remove two screws on the bottom side of notebook



Figure 2-11 Remove two screws on the rear side of notebook

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5. To remove the hinge cover, unscrew three screws. (Figure 2-12)
6. Disconnect the LCD cables from the mother board (❶) and Pull out the antenna from the KB cable's compartment (❷). Then unscrew the four screws (❸). Now you can separate the LCD ASSY. (Figure 2-13)

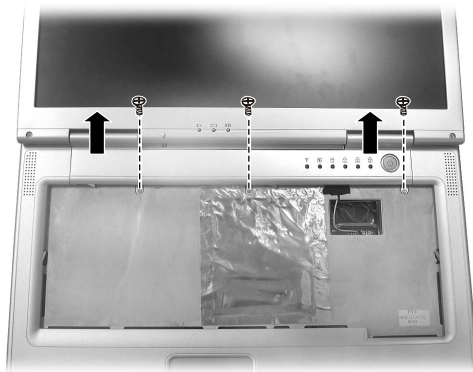


Figure 2-12 Remove the hinge cover

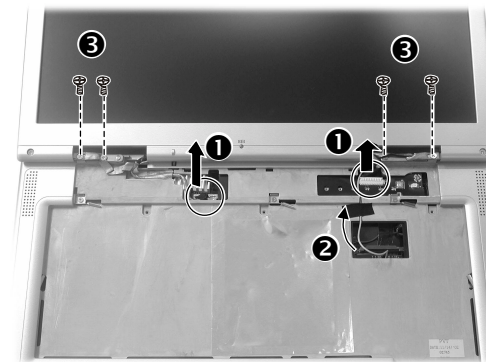


Figure 2-13 Remove the LCD ASSY

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges.
2. Reconnect the two cables to the mother board.
3. Reconnect the antenna to the wireless card. (See section 2.2.5 Reassembly)
4. Replace the hinge cover and secure with three screws.
5. Replace the keyboard and battery pack. (See sections 2.2.2 and 2.2.1 Reassembly)

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2.2.7 Inverter Board

Disassembly

1. Remove the battery pack, keyboard and LCD assembly. (See sections 2.2.1, 2.2.2 and 2.2.6 Disassembly)
2. Remove six rubber pads and six screws fastening the LCD cover. (Figure 2-14)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the cover out. Repeat the process until the cover is completely separated from the housing. .
4. To remove the inverter board on the lower part of the LCD housing , remove two screws and disconnect two cables. (Figure 2-15)



Figure 2-14 Remove LCD cover



Figure 2-15 Remove the inverter board

Reassembly

1. Reconnect the cables. Fit the inverter board back into place and secure with two screw.
2. Replace the LCD cover and secure with six screws and rubber pads.
3. Replace the LCD assembly, keyboard and battery pack. (See section 2.2.6, 2.2.2 and 2.2.1 Reassembly)

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2.2.8 LCD Panel

Disassembly

1. Remove the battery pack, keyboard, and LCD assembly. (See sections 2.2.1 to 2.2.2 and 2.2.6 Disassembly)
2. Remove the LCD cover. (See the step 1 to 3 of section 2.2.7 Disassembly)
3. Disconnect one cable from the inverter board on the lower part of the panel. (Figure 2-16)
4. Remove the four screws on two sides of the panel and four screws on the lower part of the LCD panel. (Figure 2-16)



Figure 2-16 Remove LCD panel

Reassembly

1. Fit the LCD panel back into place and secure with eight screws, and reconnect the cable to the inverter board.
2. Fit the LCD cover back into the housing and ensure inosculated well. Then replace the six screws and six rubber pads.
3. Replace the LCD assembly, keyboard, battery pack. (See section 2.2.6, 2.2.2 and 2.2.1 Reassembly)

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2.2.9 CPU

Disassembly

1. Remove the battery pack, keyboard, HDD module, CD/DVD-ROM drive and LCD assembly. (See sections 2.2.1 to 2.2.6 Disassembly)
2. Turn the four hex nuts to left to unscrew it completely. (Figure 2-17)
3. Carefully put the notebook upside down. Remove seventeen screws on the bottom of the notebook. Then detach the housing. (Figure 2-18)

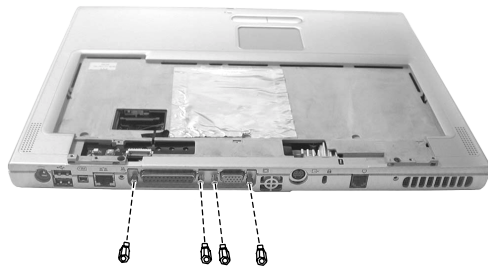


Figure 2-17 Remove the four hex nuts

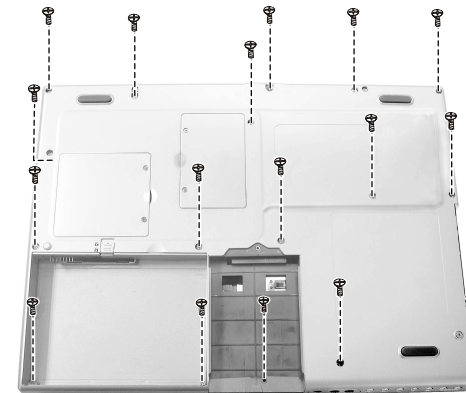


Figure 2-18 Remove the seventeen screws

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4. Remove three screws fastening the mother board ASSY. (Figure 2-19)
5. Disconnect the two speaker cables (❶); MDC wire (❷); cover switch cable (❸); MIC wire (❹); Audio cable (❺). (Figure 2-20)

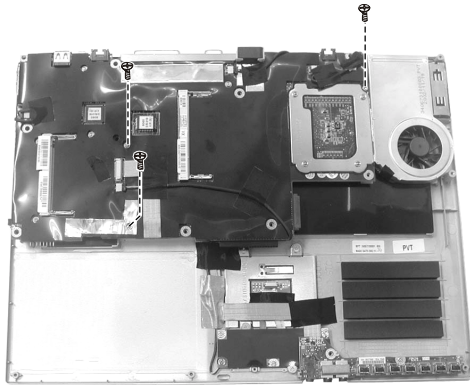


Figure 2-19 Remove the three screws

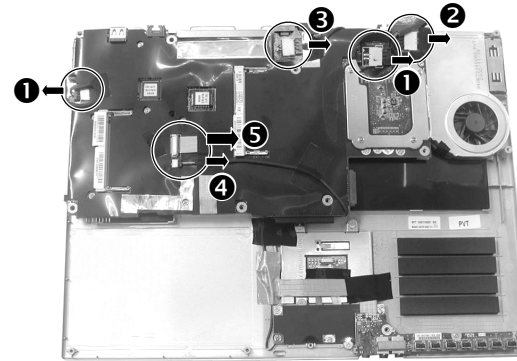


Figure 2-20 Disconnect all the cables and wires

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7. Disconnect the TP & MB cable. Now you can separate the system board ASSY. (Figure 2-21)
8. To remove the heatsink ASSY, remove four spring screws fastening the heatsink ASSY and disconnect the fan's power cord. (Figure 2-22)



Figure 2-21 Remove the system board

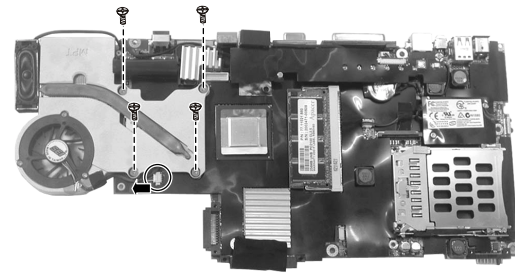


Figure 2-22 Remove the heatsink ASSY

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7. Using a flat screwdriver, rotate the lock of the CPU socket until the arrow points to the “O” position for removing the CPU. (Figure 2-23)

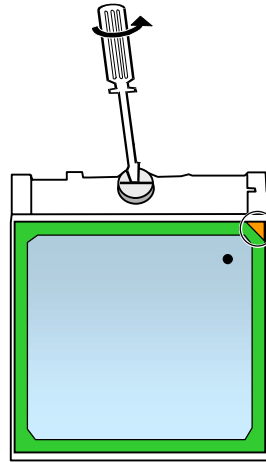


Figure 2-23 Remove the CPU

Reassembly

1. Align the arrowhead corner of the CPU with the beveled corner of the socket and insert the CPU pins into holes.
2. Use a flat screwdriver to rotate the lock of the CPU socket until the arrow points to the “L” position for securing the CPU in place.
3. Reconnect the fan’s power cord to the system board, and fit the heatsink onto the top of the CPU and secure with four screws.
4. Replace the heatsink and secure with four spring screws. Then reconnect the fan’s power cord.
5. Reconnect the TP & MB cable and then fit the mother board into place.

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6. Reconnect the two speaker cables (❶); MDC wire (❷); cover switch cable (❸); MIC wire (❹); Audio cable (❺).
7. Fasten the mother board by three screws.
8. Replace the housing and secure seventeen screws on the bottom of the notebook and four hex nuts on the rear side of notebook.
9. Fasten the housing by four hex nuts on the rear of the notebook.
10. Replace the LCD ASSY, CD/DVD-ROM, HDD, keyboard and battery pack. (See section 2.2.6 to 2.2.1 Reassembly)

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2.2.10 SO-DIMM

2.2.10.1 Extend SO-DIMM

Disassembly

1. Remove the battery pack. (See section 2.2.1 Disassembly)
2. Remove two screws locking the extend SO-DIMM compartment cover. (Figure 2-24)
3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-24)

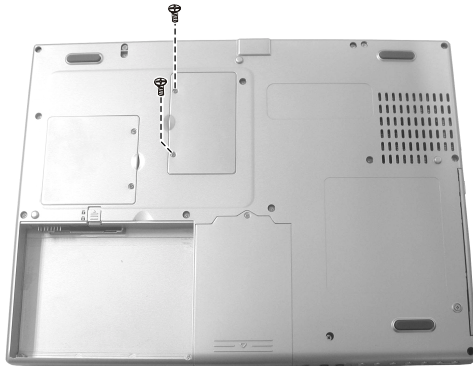


Figure 2-24 Remove the extend SO-DIMM cover

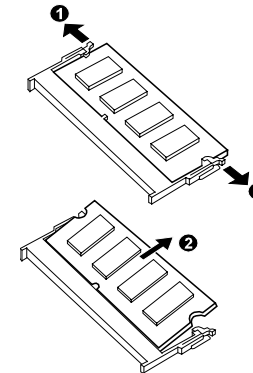


Figure 2-24 Remove the extend SO-DIMM

Reassembly

1. To install the SO-DIMM, match the SO-DIMM's notched part with the socket's projected part and firmly insert the OS-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into socket. Then replace the extend SO-DIMM compartment cover and secure with two screws.
2. Replace the battery pack. (See section 2.2.1 Reassembly)

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2.2.10 SO-DIMM

2.2.10.2 Extend SO-DIMM

Disassembly

1. Remove the mother board ASSY. (See the step 1 to 7 of section 2.2.1 Disassembly)
2. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-25)

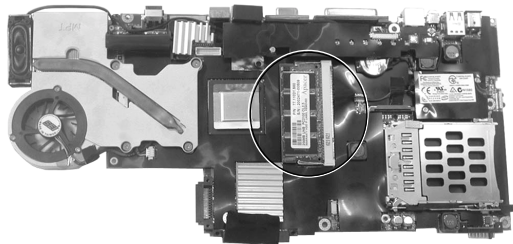


Figure 2-25 Remove the SO-DIMM

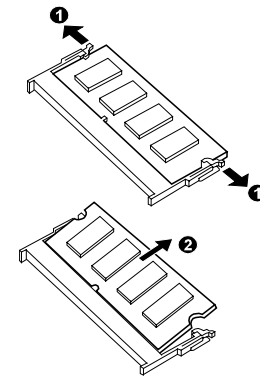


Figure 2-25 Remove the SO-DIMM

Reassembly

1. To install the SO-DIMM, match the SO-DIMM's notched part with the socket's projected part and firmly insert the OS-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into cover.
2. Assemble the notebook.

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2.2.11 Modem Card

Disassembly

1. Remove the battery pack, keyboard, HDD module, CD/DVD-ROM drive and LCD assembly. (See sections 2.2.1 to 2.2.6 Disassembly)
2. Remove the mother board ASSY. (See the step 1 to 7 of section 2.2.1 Disassembly)
3. Remove two screws fastening the modem card. (Figure 2-26)
4. Then disconnect the cable from the modem card. (Figure 2-27)

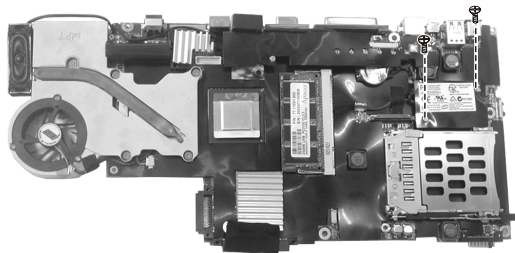


Figure 2-26 Remove two screws

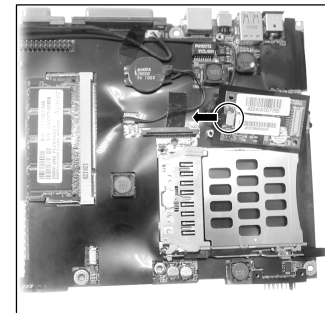


Figure 2-27 Disconnect the MDC cable

Reassembly

1. Reconnect the cable to the modem card and secure the modem card with two screws.
2. Assemble the notebook. (See previous sections Reassembly)

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2.2.12 D/D Board

Disassembly

1. Remove the battery pack, keyboard, HDD module, CD/DVD-ROM drive and LCD assembly. (See sections 2.2.1 to 2.2.6 Disassembly)
2. Remove the mother board ASSY. (See the step 1 to 7 of section 2.2.1 Disassembly)
3. Rock the D/D board to detach from the mother board. (Figure 2-28)

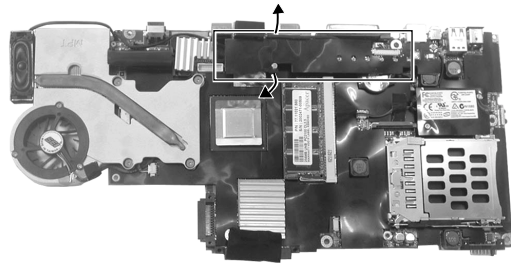


Figure 2-28 Detach the D/D Board

Reassembly

1. Insert the D/D board's pins into the connector. Then push it down and ensure every pin insert well.
2. Assemble the notebook. (See previous sections Reassembly)

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2.2.13 Mother Board

Disassembly

1. Remove the battery pack, keyboard, HDD module, CD/DVD-ROM drive and LCD assembly. (See sections 2.2.1 to 2.2.6 Disassembly)
2. Remove the heatsink, CPU, SO-DIMM, modem card, D/D board. (See section 2.2.9 to 2.2.12 Disassembly)
3. Rock the D/D board to detach from the mother board. (Figure 2-29)

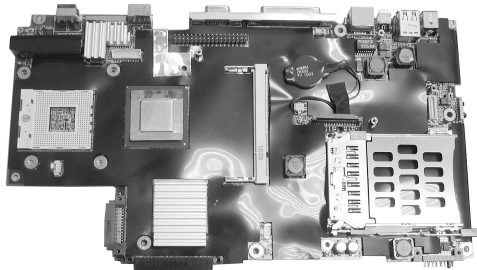


Figure 2-29 Detach the mother Board

Reassembly

1. Replace the D/D Board, modem card, CPU, heatsink. (See section 2.2.12 to 2.2.9 Reassembly)
2. Assemble the notebook. (See previous sections Reassembly)

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2.2.14 Audio Board

Disassembly

1. Remove the battery pack, keyboard, HDD module, CD/DVD-ROM drive and LCD assembly. (See sections 2.2.1 to 2.2.6 Disassembly)
2. Remove the mother board ASSY. (See the step 1 to 7 of section 2.2.1 Disassembly)
3. Remove two screws fastening the audio board and release the cable. (Figure 2-30, 2-31)

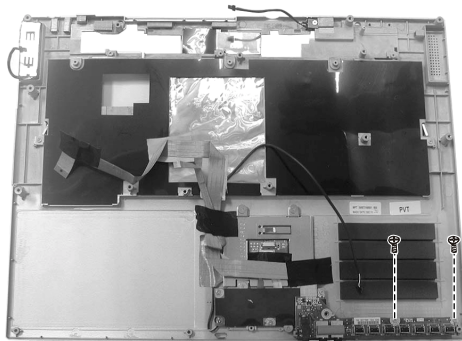


Figure 2-30 Remove the audio board

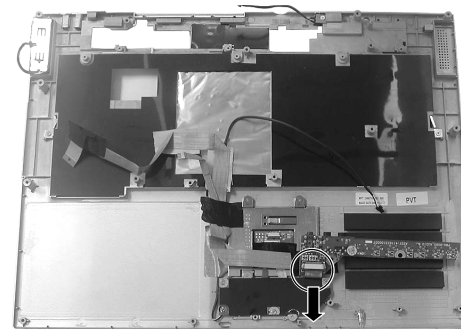


Figure 2-31 Disconnect the cable

Reassembly

1. Reconnect the cables to the audio board.
2. Replace the audio board and secure with two screws.
3. Assemble the notebook. (See previous sections Reassembly)

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2.2.15 Touch Pad Board

Disassembly

1. Remove the battery pack, keyboard, HDD module, CD/DVD-ROM drive and LCD assembly. (See sections 2.2.1 to 2.2.6 Disassembly)
2. Remove the mother board ASSY. (See the step 1 to 7 of section 2.2.1 Disassembly)
3. Remove the audio board. (See section 2.2.13 Disassembly)
4. Remove the three screws to lift up the touch pad board. (Figure 2-32)
5. Disconnect the TP & MB and the touch pad cables. (Figure 2-33)

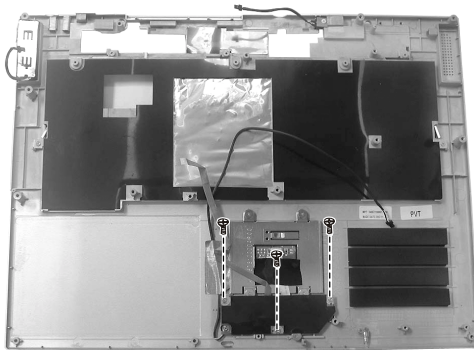


Figure 2-32 Remove the touch pad board

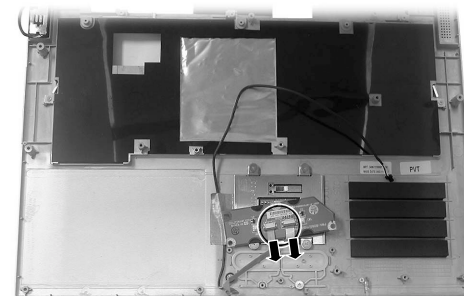


Figure 2-33 Disconnect two cables

Reassembly

1. Reconnect the TP & MB and the touch pad cables to the board
2. Replace the touch pad board and secure with three screws.
3. Assemble the notebook. (See previous sections Reassembly)

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2.2.16 Touch Pad Module

Disassembly

1. Remove the battery pack, keyboard, HDD module, CD/DVD-ROM drive and LCD assembly. (See sections 2.2.1 to 2.2.6 Disassembly)
2. Remove the mother board ASSY. (See the step 1 to 7 of section 2.2.1 Disassembly)
3. Remove the audio board and touch pad board. (See sections 2.2.13 and 2.2.14 Disassembly)
4. Remove four screws fastening the touch pad module and disconnect the touch pad's cable to lift up the touch pad module. (Figure 2-33)

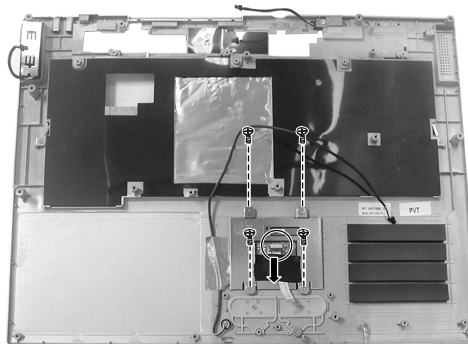


Figure 2-34 Remove the top mother board

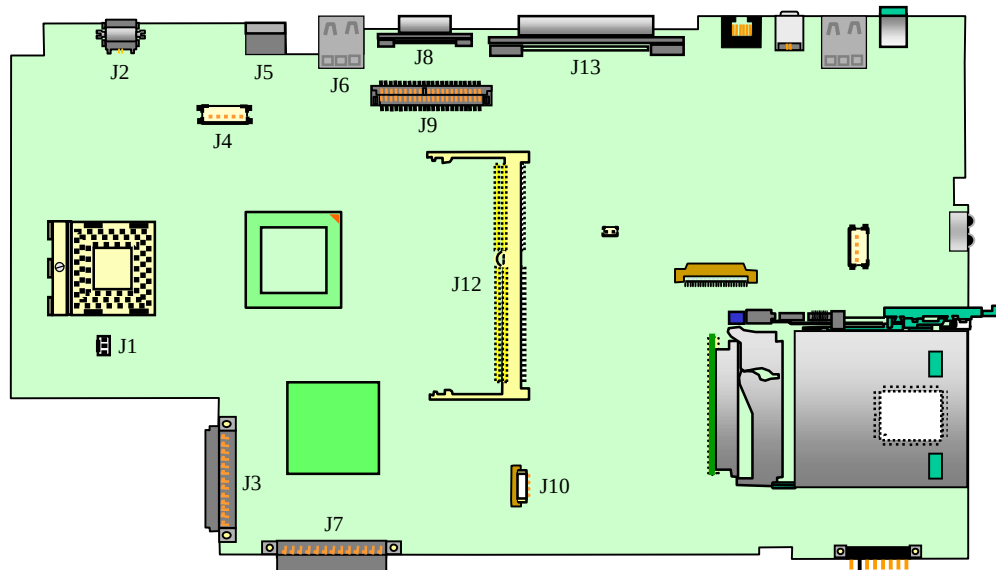
Reassembly

1. Replace the touch pad module and bracket and secure with four screws.
2. Reconnect the cables to the board.
3. Assemble the notebook. (See previous sections Reassembly)

8060B N/B Maintenance

3. Definition & Location of Connectors / Switches

3.1 Main Board (Side A) – 1



- ✚ J1 : FAN Connector
- ✚ J2 : RJ11 Connector
- ✚ J3 : Secondary EIDE Connector
- ✚ J4 : LCD Connector
- ✚ J5 : S-Video Connector
- ✚ J6 : USB Port Connector
- ✚ J7 : Primary EIDE Connector
- ✚ J8 : External VGA Connector
- ✚ J9 : DC to DC Board Connector
- ✚ J10 : Touch-pad Connector
- ✚ J12 : DDR SO-DIMM Module Socket
- ✚ J13 : Parallel Port Connector

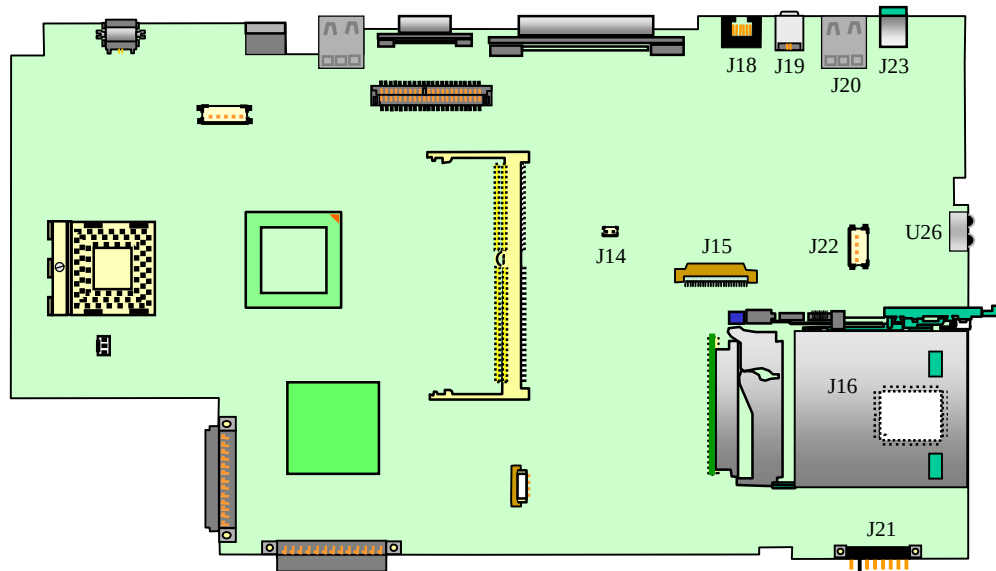
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3. Definition & Location of Connectors/ Switches

3.1 Main Board (Side A) – 2

----- Continued to previous page -----

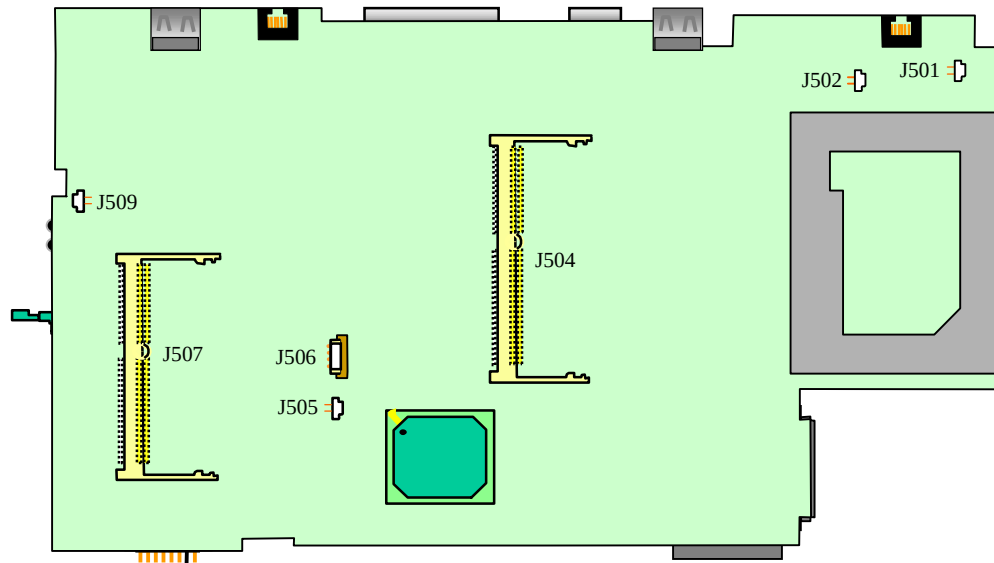


- ✦ J14 : RTC Battery Connector
- ✦ J15 : Internal Keyboard Connector
- ✦ J16 : PCMCIA Card Bus Socket
- ✦ J18 : LAN (RJ45) Connector
- ✦ J19 : IEEE1394 Connector
- ✦ J20 : USB Port Connector
- ✦ J21 : Battery Connector
- ✦ J22 : Modem Daughter Board (MDC) Connector
- ✦ J23 : AC Power Jack
- ✦ U26 : FIR Module

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3. Definition & Location of Connectors/ Switches

3.1 Main Board (Side B)

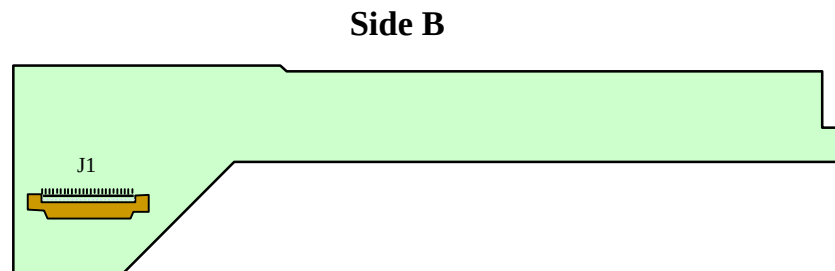
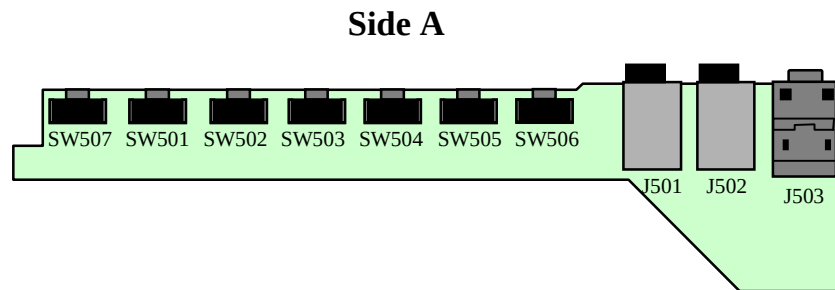


- ✚ J501 : MDC Jump Wire Connector
- ✚ J502 : Left Internal Speaker Connector
- ✚ J504 : DDR SO-DIMM Module Socket
- ✚ J505 : Internal Microphone Connector
- ✚ J506 : Audio DJ Board Connector
- ✚ J507 : Mini PCI Socket
- ✚ J509 : Right Internal Speaker Connector

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3. Definition & Location of Connectors / Switches

3.2 Audio DJ Board

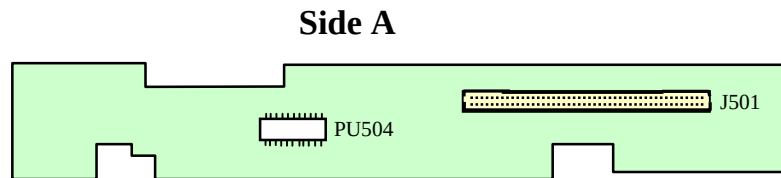


- ✦ SW501 : Volume Up Switch
- ✦ SW502 : STOP/EJECT Switch
- ✦ SW503 : PLAY/PAUSE Switch
- ✦ SW504 : FF Switch
- ✦ SW505 : RW Switch
- ✦ SW506 : ADJ Button
- ✦ SW507 : Volume Down
- ✦ J501 : External Microphone Jack
- ✦ J502 : Line In Jack
- ✦ J503 : Line Out Jack
- ✦ J1 : Audio DJ Board Connector

8060B N/B Maintenance

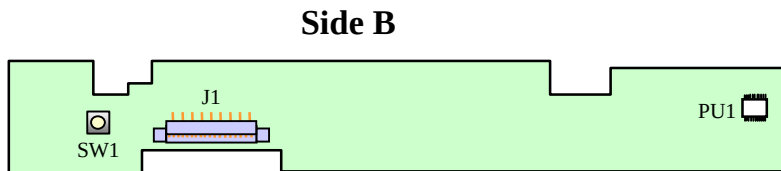
3. Definition & Location of Connectors / Switches

3.3 DC to DC Board



⊕ J501 : DC to DC Board Connector

⊕ PU504 : LTC3707 (DDR_2.5V) DC to DC Converter



⊕ J1 : Inverter Board Connector

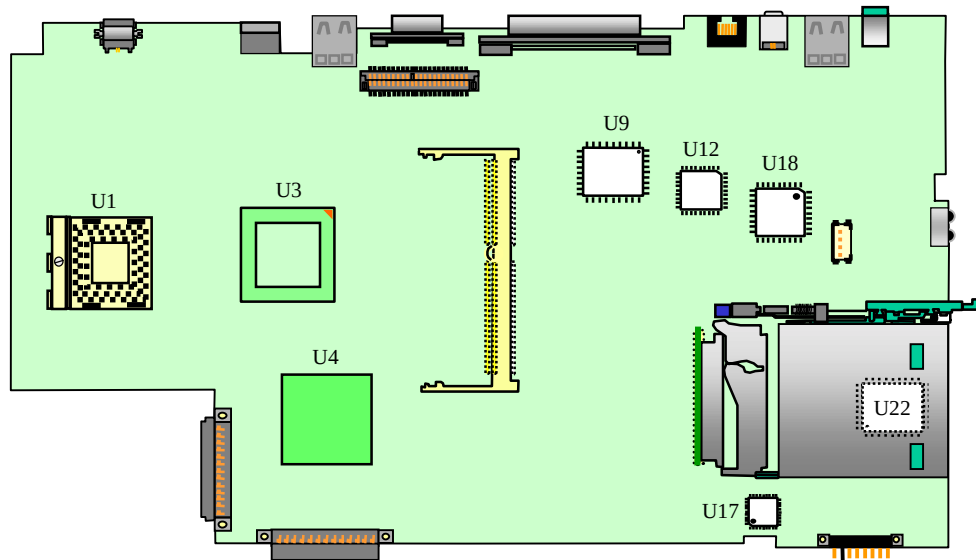
⊕ SW1 : Power Switch

⊕ PU1 : LP2996 (REF_1.25V) DC to DC Converter

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4. Definition & Location of Major Components

4.1 Main Board (Side A)

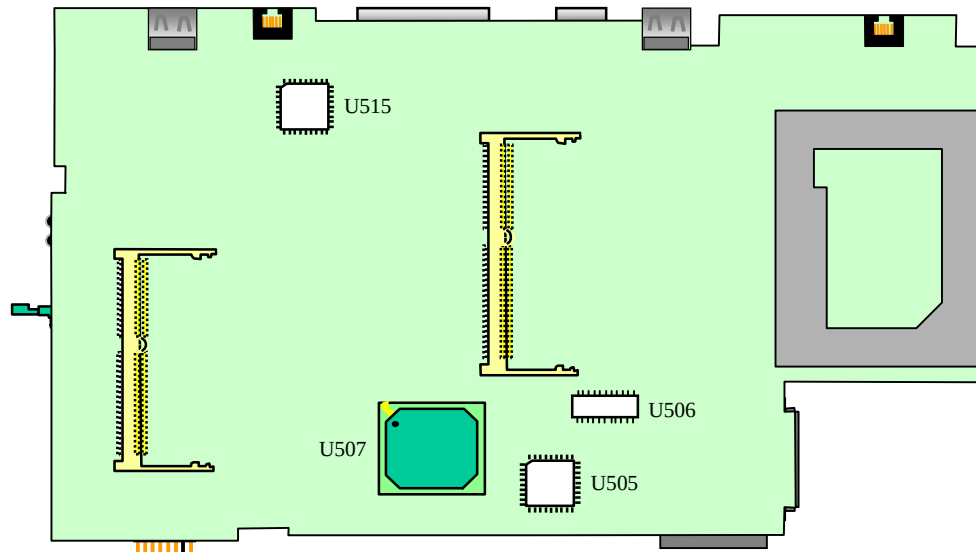


- ✦ U1 : Intel Pentium M Processor
- ✦ U3 : Intel 82855GM Memory Controller Hub (Odem)
- ✦ U8 : NVIDIA NV18M VGA Controller
- ✦ U9 : RTL8101L LAN Controller
- ✦ U12 : Flash ROM (BIOS)
- ✦ U17 : ALC202 Audio CODEC
- ✦ U18 : H8/F3437 Micro Controller
- ✦ U22 : PCI4510 PCMCIA &1394 Controller

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4. Definition & Location of Major Components

4.1 Main Board (Side B)



- ✦ U505 : OZ165 Audio DJ Controller
- ✦ U506 : ICS950810 Clock Generator
- ✦ U507 : Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)
- ✦ U515 : PC87393 Super I/O Controller

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5. Pin Descriptions of Major Components

5.1 Intel Pentium M Processor

Signal Name	Type	Description						
A[31:3]#	I/O	A[31:3]# (Address) define a 2 32 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Intel Pentium M processor system bus. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.						
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.						
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.						
ADSTB[1:0]#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strokes are associated with signals as shown below. <table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr><tr><td>A[31:17]#</td><td>ADSTB[1]#</td></tr></table>	Signals	Associated Strobe	REQ[4:0]#, A[16:3]#	ADSTB[0]#	A[31:17]#	ADSTB[1]#
Signals	Associated Strobe							
REQ[4:0]#, A[16:3]#	ADSTB[0]#							
A[31:17]#	ADSTB[1]#							
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.						
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.						
BPM[2:0]# BPM[3]	O I/O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel Pentium M processor system bus agents. This includes debug or performance monitoring tools.						

Signal Name	Type	Description															
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of both processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.															
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the Intel Pentium M processor (Symmetric Agent) and the MCH-M (High Priority Agent) of the Intel 855PM or Intel 855GM chipset.															
COMPP3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more implementation details.															
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. <table border="1"> <caption>Quad-Pumped Signal Groups</caption> <thead> <tr> <th>Data Group</th><th>DSTBN#/DSTBP#</th><th>DINV#</th></tr> </thead> <tbody> <tr> <td>D[15:0]#</td><td>0</td><td>0</td></tr> <tr> <td>D[31:16]#</td><td>1</td><td>1</td></tr> <tr> <td>D[47:32]#</td><td>2</td><td>2</td></tr> <tr> <td>D[63:48]#</td><td>3</td><td>3</td></tr> </tbody> </table> Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.	Data Group	DSTBN#/DSTBP#	DINV#	D[15:0]#	0	0	D[31:16]#	1	1	D[47:32]#	2	2	D[63:48]#	3	3
Data Group	DSTBN#/DSTBP#	DINV#															
D[15:0]#	0	0															
D[31:16]#	1	1															
D[47:32]#	2	2															
D[63:48]#	3	3															
DBR#	O	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect. DBR# is not a processor signal.															

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5.1 Intel Pentium M Processor

Signal Name	Type	Description										
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both processor system bus agents.										
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both processor system bus agents.										
DINV[3:0]#	I/O	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. DINV[3:0]# Assignment To Data Bus <table><tr><th>Bus Signal</th><th>Data Bus Signals</th></tr><tr><td>DINV[3]#</td><td>D[63:48]#</td></tr><tr><td>DINV[2]#</td><td>D[47:32]#</td></tr><tr><td>DINV[1]#</td><td>D[31:16]#</td></tr><tr><td>DINV[0]#</td><td>D[15:0]#</td></tr></table>	Bus Signal	Data Bus Signals	DINV[3]#	D[63:48]#	DINV[2]#	D[47:32]#	DINV[1]#	D[31:16]#	DINV[0]#	D[15:0]#
Bus Signal	Data Bus Signals											
DINV[3]#	D[63:48]#											
DINV[2]#	D[47:32]#											
DINV[1]#	D[31:16]#											
DINV[0]#	D[15:0]#											
DPSLP#	I	DPSLP# when asserted on the platform causes the processor to transition from the Sleep state to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH4-M component and also connects to the MCH-M component of the Intel 855PM or Intel 855GM chipset.										
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both processor system bus agents.										
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. <table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>D[15:0]#, DINV[0]#</td><td>DSTBN[0]#</td></tr><tr><td>D[31:16]#, DINV[1]#</td><td>DSTBN[1]#</td></tr><tr><td>D[47:32]#, DINV[2]#</td><td>DSTBN[2]#</td></tr><tr><td>D[63:48]#, DINV[3]#</td><td>DSTBN[3]#</td></tr></table>	Signals	Associated Strobe	D[15:0]#, DINV[0]#	DSTBN[0]#	D[31:16]#, DINV[1]#	DSTBN[1]#	D[47:32]#, DINV[2]#	DSTBN[2]#	D[63:48]#, DINV[3]#	DSTBN[3]#
Signals	Associated Strobe											
D[15:0]#, DINV[0]#	DSTBN[0]#											
D[31:16]#, DINV[1]#	DSTBN[1]#											
D[47:32]#, DINV[2]#	DSTBN[2]#											
D[63:48]#, DINV[3]#	DSTBN[3]#											
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. <table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>D[15:0]#, DINV[0]#</td><td>DSTBP[0]#</td></tr><tr><td>D[31:16]#, DINV[1]#</td><td>DSTBP[1]#</td></tr><tr><td>D[47:32]#, DINV[2]#</td><td>DSTBP[2]#</td></tr><tr><td>D[63:48]#, DINV[3]#</td><td>DSTBP[3]#</td></tr></table>	Signals	Associated Strobe	D[15:0]#, DINV[0]#	DSTBP[0]#	D[31:16]#, DINV[1]#	DSTBP[1]#	D[47:32]#, DINV[2]#	DSTBP[2]#	D[63:48]#, DINV[3]#	DSTBP[3]#
Signals	Associated Strobe											
D[15:0]#, DINV[0]#	DSTBP[0]#											
D[31:16]#, DINV[1]#	DSTBP[1]#											
D[47:32]#, DINV[2]#	DSTBP[2]#											
D[63:48]#, DINV[3]#	DSTBP[3]#											

Signal Name	Type	Description
DPWR#	I	DPWR# is a control signal from the Intel 855PM and Intel 855GM chipsets used to reduce power on the Intel Pentium M data bus input buffers.
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 80387 coprocessor, and is included for compatibility with systems using MS-DOS* type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.
GTLREF	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP} . GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.
HIT# HITM#	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of both processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.

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5.1 Intel Pentium M Processor

Signal Name	Type	Description
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power on Reset vector configured during power on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST)
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space and used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	O	PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal may require voltage translation on the motherboard.
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (Deep Sleep and Deeper Sleep).

Signal Name	Type	Description
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal as a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout the boundary scan operation.
ITP_CLK[1:0]	I	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects. These are not processor signals.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications. On observing active RESET#, both system bus agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both processor system bus agents.
RSVD	-	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.

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5.1 Intel Pentium M Processor

Signal Name	Type	Description
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3	I	TEST1, TEST2, and TEST3 must be left unconnected but should have a stuffing option connection to V SS separately using 1-k, pull-down resistors.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both system bus agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.

Signal Name	Type	Description
VCC	I	Processor core power supply.
VCCA[3:0]	I	VCCA provides isolated power for the internal processor core PLL's.
VCCP	I	Processor I/O Power Supply.
VCCQ[1:0]	I	Quiet power supply for on die COMP circuitry. These pins should be connected to VCCP on the motherboard. However, these connections should enable addition of decoupling on the VCCQ lines if necessary.
VCCSENSE	O	VCCSENSE is an isolated low impedance connection to processor core power (VCC). It can be used to sense or measure power near the silicon with little noise.
VID[5:0]	O	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Pentium M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations.
VSSSENSE	O	VSSSENSE is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise.

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5.2 Intel 82855GM Memory Controller Hub (Odem)

Host Interface Signals

Signal Name	Type	Description
ADS#	I/O AGTL+	Address Strobe: The system bus owner asserts ADS# to indicate the first of two cycles of a request phase. The GMCH can assert this signal for snoop cycles and interrupt messages.
BNR#	I/O AGTL+	Block Next Request: Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O AGTL+	Bus Priority Request: The GMCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	I/O AGTL+	Bus Request 0#: The GMCH pulls the processor bus BREQ0# signal low during CPURST#. The signal is sampled by the processor on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 BCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 BCLKs. BREQ0# should be tristated after the hold time requirement has been satisfied. During regular operation, the GMCH will use BREQ0# as an early indication for PSB Address and Ctl input buffer and sense amp activation.
CPURST#	O AGTL+	CPU Reset: The CPURST# pin is an output from the GMCH. The GMCH asserts CPURST# while RESET# (PCIRST# from ICH4-M) is asserted and for approximately 1 ms after RESET# is deasserted. The CPURST# allows the processor to begin execution in a known state. Note that the ICH4-M must provide CPU strap set-up and hold-times around CPURST#. This requires strict synchronization between GMCH, CPURST# deassertion and ICH4-M driving the straps.
DBSY#	I/O AGTL+	Data Bus Busy: Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	Defer: GMCH will generate a deferred response as defined by the rules of the GMCH's Dynamic Defer policy. The GMCH will also use the DEFER# signal to indicate a CPU retry response.
DPSLP#	I CMOS	Deep Sleep #: This signal comes from the ICH4-M device, providing an indication of C3 and C4 state control to the CPU. Deassertion of this signal is used as an early indication for C3 and C4 wake up (to active HPLL). Note that this is a low-voltage CMOS buffer operating on the PSB VTT power plane.
HD[63:0]#	I/O AGTL+	Host Data: These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus.

Host Interface Signals Continue

Signal Name	Type	Description										
DINV[3:0]#	I/O AGTL+	Dynamic Bus Inversion: Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. <table><tr><th>DINV#</th><th>Data Bits</th></tr><tr><td>DNIV[3]#</td><td>HD[63:48]#</td></tr><tr><td>DNIV[2]#</td><td>HD[47:32]#</td></tr><tr><td>DINV[1]#</td><td>HD[31:16]#</td></tr><tr><td>DINV[0]#</td><td>HD[15:0]#</td></tr></table>	DINV#	Data Bits	DNIV[3]#	HD[63:48]#	DNIV[2]#	HD[47:32]#	DINV[1]#	HD[31:16]#	DINV[0]#	HD[15:0]#
DINV#	Data Bits											
DNIV[3]#	HD[63:48]#											
DNIV[2]#	HD[47:32]#											
DINV[1]#	HD[31:16]#											
DINV[0]#	HD[15:0]#											
HA[31:0]#	I/O AGTL+	Host Address Bus: HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The GMCH drives HA[31:3]# during snoop cycles on behalf of Hub Interface. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.										
HADSB[1:0]#	I/O AGTL+	Host Address Strobe: HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. <table><tr><th>Strobe</th><th>Address Bits</th></tr><tr><td>HADSTB[0]#</td><td>HA[16:3]#, HREQ[4:0]#</td></tr><tr><td>HADSTB[1]#</td><td>HA[31:17]#</td></tr></table>	Strobe	Address Bits	HADSTB[0]#	HA[16:3]#, HREQ[4:0]#	HADSTB[1]#	HA[31:17]#				
Strobe	Address Bits											
HADSTB[0]#	HA[16:3]#, HREQ[4:0]#											
HADSTB[1]#	HA[31:17]#											
DRDY#	I/O AGTL+	Data Ready: Asserted for each cycle that data is transferred.										
HDSTBP[3:0]# HDSTBN[3:0]#	I/O AGTL+	Differential Host Data Strokes: The differential source synchronous strobes are used to transfer HD[63:0]# and DINV[3:0]# at the 4x transfer rate. <table><tr><th>Strobe</th><th>Data Bits</th></tr><tr><td>HDSTBP[3]#, HDSTBN[3]#</td><td>HD[63:48]#, DINV[3]#</td></tr><tr><td>HDSTBP[2]#, HDSTBN[2]#</td><td>HD[47:32]#, DINV[2]#</td></tr><tr><td>HDSTBP[1]#, HDSTBN[1]#</td><td>HD[31:16]#, DINV[1]#</td></tr><tr><td>HDSTBP[0]#, HDSTBN[0]#</td><td>HD[15:0]#, DINV[0]#</td></tr></table>	Strobe	Data Bits	HDSTBP[3]#, HDSTBN[3]#	HD[63:48]#, DINV[3]#	HDSTBP[2]#, HDSTBN[2]#	HD[47:32]#, DINV[2]#	HDSTBP[1]#, HDSTBN[1]#	HD[31:16]#, DINV[1]#	HDSTBP[0]#, HDSTBN[0]#	HD[15:0]#, DINV[0]#
Strobe	Data Bits											
HDSTBP[3]#, HDSTBN[3]#	HD[63:48]#, DINV[3]#											
HDSTBP[2]#, HDSTBN[2]#	HD[47:32]#, DINV[2]#											
HDSTBP[1]#, HDSTBN[1]#	HD[31:16]#, DINV[1]#											
HDSTBP[0]#, HDSTBN[0]#	HD[15:0]#, DINV[0]#											
HIT#	I/O AGTL+	Hit: Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.										
HITM#	I/O AGTL+	Hit Modified: Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.										
HLOCK#	I/O AGTL+	Host Lock: All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no Hub Interface snoopable access to System Memory is allowed when HLOCK# is asserted by the CPU.										

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5.2 Intel 82855GM Memory Controller Hub (Odem)

Host Interface Signals (Continued)

Signal Name	Type	Description																		
HREQ[4:0]#	I/O AGTL+	Host Request Command: Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.																		
HTRDY#	O AGTL+	Host Target Ready: Indicates that the target of the processor transaction is able to enter the data transfer phase.																		
RS[2:0]#	O AGTL+	Response Status: Indicates type of response according to the following table: <table><tr><th><u>RS[2:0]</u></th><th><u>Response type</u></th></tr><tr><td>000</td><td>Idle state</td></tr><tr><td>001</td><td>Retry response</td></tr><tr><td>010</td><td>Deferred response</td></tr><tr><td>011</td><td>Reserved (not driven by MCH-M)</td></tr><tr><td>100</td><td>Hard Failure (not driven by MCH-M)</td></tr><tr><td>101</td><td>No data response</td></tr><tr><td>110</td><td>Implicit Write back</td></tr><tr><td>111</td><td>Normal data response</td></tr></table>	<u>RS[2:0]</u>	<u>Response type</u>	000	Idle state	001	Retry response	010	Deferred response	011	Reserved (not driven by MCH-M)	100	Hard Failure (not driven by MCH-M)	101	No data response	110	Implicit Write back	111	Normal data response
<u>RS[2:0]</u>	<u>Response type</u>																			
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DDR SDRAM Interface Signals

Signal Name	Type	Description
SCS [3:0]#	O SSTL_2	Chip Select: These pins select the particular DDR SDRAM components during the active state. Note: There is one SCS# per DDR-SDRAM Physical SO-DIMM device row. These signals can be toggled on every rising System Memory Clock edge.
SMA[12:0]	O SSTL_2	Multiplexed Memory Address: These signals are used to provide the multiplexed row and column address to DDR SDRAM.
SBA[1:0]	O SSTL_2	Bank Select (Memory Bank Address): These signals define which banks are selected within each DDR SDRAM row. The SMA and SBA signals combine to address every possible location within a DDR SDRAM device.
SRAS#	O SSTL_2	DDR Row Address Strobe: SRAS# may be heavily loaded and requires two DDR SDRAM clock cycles for setup time to the DDR SDRAMs. Used with SCAS# and SWE# (along with SCS#) to define the System Memory commands.
SCAS#	O SSTL_2	DDR Column Address Strobe: SCAS# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs. Used with SRAS# and SWE# (along with SCS#) to define the System Memory commands.

DDR SDRAM Interface Signals Continue

Signal Name	Type	Description
SWE#	O SSTL_2	Write Enable: Used with SCAS# and SRAS# (along with SCS#) to define the DDR SDRAM commands. SWE# is asserted during writes to DDR SDRAM. SWE# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs.
SDQ[71:0]	I/O SSTL_2	Data Lines: These signals are used to interface to the DDR SDRAM data bus. NOTE: ECC error detection is supported by the SDQ[71:64] signals.
SDQS[8:0]	I/O SSTL_2	Data Strobes: Data strobes are used for capturing data. During writes, SDQS is centered on data. During reads, SDQS is edge aligned with data. The following list matches the data strobe with the data bytes. There is an associated data strobe (DQS) for each data signal (DQ) and check bit (CB) group. SDQS[7] -> SDQ[63:56] SDQS[6] -> SDQ[55:48] SDQS[5] -> SDQ[47:40] SDQS[4] -> SDQ[39:32] SDQS[3] -> SDQ[31:24] SDQS[2] -> SDQ[23:16] SDQS[1] -> SDQ[15:8] SDQS[0] -> SDQ[7:0] NOTE: ECC error detection is supported by the SDQS[8] signal.
SCKE[3:0]	O SSTL_2	Clock Enable: These pins are used to signal a self-refresh or power down command to the DDR SDRAM array when entering system suspend. SCKE is also used to dynamically power down inactive DDR SDRAM rows. There is one SCKE per DDR SDRAM row. These signals can be toggled on every rising SCK edge.
SMAB[5,4,2,1]	O SSTL_2	Memory Address Copies: These signals are identical to SMA[5,4,2,1] and are used to reduce loading for selective CPC(clock-per-command). These copies are not inverted.
SDM[8:0]	O SSTL_2	Data Mask: When activated during writes, the corresponding data groups in the DDR SDRAM are masked. There is one SDM for every eight data lines. SDM can be sampled on both edges of the data strobes. NOTE: ECC error detection is supported by the SDM[8] signal.
RCVENOUT#	O SSTL_2	Clock Output: Reserved, NC.
RCVENIN#	I SSTL_2	Clock Input: Reserved, NC.

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5.2 Intel 82855GM Memory Controller Hub (Odem)

Hub Interface Signals

Signal Name	Type	Description
HI_[10:0]	I/O Hub	Packet Data: Data signals used for HI read and write operations.
HI_STB	I/O Hub	Packet Strobe: One of two differential strobe signals used to transmit or receive packet data over HI.
HI_STB#	I/O Hub	Packet Strobe Complement: One of two differential strobe signals used to transmit or receive packet data over HI.

Clock Signals

Signal Name	Type	Description
Host Processor Clocking		
BC.LK BCLK#	I CMOS	Differential Host Clock In: These pins receive a buffered host clock from the external clock synthesizer. This clock is used by all of the GMCH logic that are in the Host clock domain (Host, Hub and System Memory). The clock is also the reference clock for the graphics core PLL. This is a low voltage differential input.
System Memory Clocking		
SCK[5:0]	O SSTL_2	Differential DDR SDRAM Clock: SCK and SCK# pairs are differential clock outputs. The crossing of the positive edge of SCK and the negative edge of SCK# is used to sample the address and control signals on the DDR SDRAM. There are 3 pairs to each SO-DIMM. NOTE: ECC error detection is supported by the SCK[2] and SCK[5] signals.
SCK[5:0]#	O SSTL_2	Complementary Differential DDR SDRAM Clock: These are the complimentary differential DDR SDRAM clock signals. NOTE: ECC error detection is supported by the SCK[2]# and SCK[5]# signals.
DVO/Hub Input Clocking		
GCLKIN	I CMOS	Input Clock: 66-MHz, 3.3-V input clock from external buffer DVO/Hub Interface.
DVO Clocking		
DVOBC.LK DVOBCLK#	O DVO	Differential DVO Clock Output: These pins provide a differential pair reference clock that can run up to 165-MHz. DVOBCLK corresponds to the primary clock out. DVOBCLK# corresponds to the primary complementary clock out. DVOBCLK and DVOBCLK# should be left as NC ("Not Connected") if the DVO B port is not implemented.

Clock Signals Continue

Signal Name	Type	Description
DVOCC.LK DVOCCCLK#	O DVO	Differential DVO Clock Output: These pins provide a differential pair reference clock that can run up to 165-MHz. DVOCCCLK corresponds to the primary clock out. DVOCCCLK# corresponds to the primary complementary clock out. DVOCCCLK and DVOCCCLK# should be left as NC ("Not Connected") if the DVO C port is not implemented.
DVOBCCLKINT	I DVO	DVOBC Pixel Clock Input/Interrupt: This signal may be selected as the reference input to either dot clock PLL (DPLL) or may be configured as an interrupt input. A TV-out device can provide the clock reference. The maximum input frequency for this signal is 85 -MHz. DVOBC Pixel Clock Input: When selected as the dot clock PLL (DPLL) reference input, this clock reference input supports SSC clocking for DVO LVDS devices. DVOBC Interrupt: When configured as an interrupt input, this interrupt can support either DVOB or DVOC. DVOBCCLKINT needs to be pulled down if the signal is NOT used.
DPMS	I DVO	Display Power Management Signaling: This signal is used only in mobile systems to act as the DREFCLK in certain power management states(i.e. Display Power Down Mode); DPMS Clock is used to refresh video during S1-M. Clock Chip is powered down in S1-M. DPMS should come from a clock source that runs during
DAC Clocking		
DREFCLK	I LVTTTL	Display Clock Input: This pin is used to provide a 48-MHz input clock to the Display PLL that is used for 2D/Video and DAC.
LVDS LCK Flat Panel Clocking		
DREFSSCLK	I LVTTTL	Display SSC Clock Input: This pin provides a 48-MHz or 66-MHz input clock (SSC or non-SSC) to the Display PLL B.

Dedicated LVDS LCD Flat Panel Interface Signals

Signal Name	Type	Voltage	Description
ICLKAP	O LVDS	1.25 V± 225 mV	Channel A differential clock pair output (true): 245-800 MHz
ICLKAM	O LVDS	1.25 V± 225 mV	Channel A differential clock pair output (compliment): 245-800 MHz.
IYAP[3:0]	O LVDS	1.25 V± 225 mV	Channel A differential data pair 3:0 output (true): 245-800 MHz.
IYAM[3:0]	O LVDS	1.25 V± 225 mV	Channel A differential data pair 3:0 output (compliment): 245-800 MHz.

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5.2 Intel 82855GM Memory Controller Hub (Odem)

Dedicated LVDS LCD Flat Panel Interface Signals (Continued)

Signal Name	Type	Voltage	Description
ICLKBP	O LVDS	1.25 V± 225 mV	Channel B differential clock pair output (true): 245-800 MHz.
ICLKBM	O LVDS	1.25 V± 225 mV	Channel B differential clock pair output (compliment): 245-800 MHz.
IYBP[3:0]	O LVDS	1.25 V± 225 mV	Channel B differential data pair 3:0 output (true): 245-800 MHz.
IYBM[3:0]	O LVDS	1.25 V± 225 mV	Channel B differential data pair 3:0 output (compliment): 245-800 MHz.

Digital Video Output B (DVOB) Port Signals

Signal Name	Type	Description
DVOBD[11:0]	O DVO	DVOB Data: This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOBCLK and DVOBCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the lower 12-bits of pixel data. DVOBD[11:0] should be left as left as NC ("Not Connected") if not used.
DVOBHSYNC	O DVO	Horizontal Sync: HSYNC signal for the DVOB interface. DVOBHSYNC should be left as left as NC ("Not Connected") if not used.
DVOBVSYSN	O DVO	Vertical Sync: VSYNC signal for the DVOB interface. DVOBVSYSN should be left as left as NC ("Not Connected") if the signal is NOT used when using internal graphics device.
DVOBBLANK#	O DVO	Flicker Blank or Border Period Indication: DVOBBLANK# is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOBBLANK# should be left as left as NC ("Not Connected") if not used.
DVOBFLDSTL	I DVO	TV Field and Flat Panel Stall Signal. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOB TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOB Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOBFLDSTL needs to be pulled down if not used.

Digital Video Output C (DVOC) Port Signals

Signal Name	Type	Description
DVOC[11:0]	O DVO	DVOC Data: This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOCCLK and DVOCCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the upper 12-bits of pixel data. DVOC[11:0] should be left as left as NC ("Not Connected") if not used.
DVOCHSYNC	O DVO	Horizontal Sync: HSYNC signal for the DVOC interface. DVOCHSYNC should be left as left as NC ("Not Connected") if not used.
DVOCVSYNC	O DVO	Vertical Sync: VSYNC signal for the DVOC interface. DVOCVSYNC should be left as left as NC ("Not Connected") if the signal is NOT used when using internal graphics device.
DVOCBLANK#	O DVO	Flicker Blank or Border Period Indication: DVOCBLANK# is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOCBLANK# should be left as left as NC ("Not Connected") if not used.
DVOCFLDSTL	I DVO	TV Field and Flat Panel Stall Signal. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOC TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOC Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOCFLDSTL needs to be pulled down if not used.

DVOB and DVOC Port Common Signals

Signal Name	Type	Description
DVOBCINTR#	I DVO	DVOBC Interrupt: This pin is used to signal an interrupt, typically used to indicate a hot plug or unplug of a digital display.
ADDID[7:0]	I DVO	ADDID[7:0]: These pins are used to communicate to the Video BIOS when an external device is interfaced to the DVO port. Note: Bit[7] needs to be strapped low when an on-board DVO device is present. The other pins should be left as NC.
DVODETECT	I DVO	DVODETECT: This strapping signal indicates to the GMCH whether a DVO device is present or not. When a DVO device is connected, then DVODETECT = 0.

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5.2 Intel 82855GM Memory Controller Hub (Odem)

Analog CRT Display Signals

Signal Name	Type	Description
VSYNC	O CMOS	CRT Vertical Synchronization: This signal is used as the vertical sync signal.
HSYNC	O CMOS	CRT Horizontal Synchronization: This signal is used as the horizontal sync signal.
RED	O Analog	Red (Analog Video Output): This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-ohm equivalent load on each pin (e.g., 75-ohm resistor on the board, in parallel with the 75-ohm. CRT load).
RED#	O Analog	Red# (Analog Output): Tied to ground.
GREEN	O Analog	Green (Analog Video Output): This signal is a CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5-ohm equivalent load on each pin (e.g., 75-ohm resistor on the board, in parallel with the 75-ohm. CRT load).
GREEN#	O Analog	Green# (Analog Output): Tied to ground.
BLUE	O Analog	Blue (Analog Video Output) : This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-ohm equivalent load on each pin (e.g., 75- ohm resistor on the board, in parallel with the 75-ohm. CRT load).
BLUE#	O Analog	Blue# (Analog Output): Tied to ground.

GPIO Signals

GPIO I/F Total	Type	Comments
RSTIN#	I CMOS	Reset: Primary Reset, Connected to PCIRST# of ICH4-M.
PWROK	I CMOS	Power OK: Indicates that power to GMCH is stable.
AGPBUSY#	O CMOS	AGPBUSY: Output of the GMCH IGD to the ICH4-M, which indicates that certain graphics activity is taking place. It will indicate to the ACPI software not to enter the C3 state. It will also cause a C3/C4 exit if C3/C4 was being entered, or was already entered when AGPBUSY# went active. Not active when the IGD is in any ACPI state other than D0.
EXTTS_0	I CMOS	External Thermal Sensor Input: This signal is an active low input to the GMCH and is used to monitor the thermal condition around the System Memory and is used for triggering a read throttle. The GMCH can be optionally programmed to send a SERR, SCI, or SMI message to the ICH4-M upon the triggering of this signal.

GPIO Signals Continue

GPIO I/F Total	Type	Comments
LCLKCTLA	O CMOS	SSC Chip Clock Control: Can be used to control an external clock chip with SSC control.
LCLKCTLB	O CMOS	SSC Chip Data Control: Can be used to control an external clock chip for SSC control.
PANELVDDEN	O CMOS	LVDS LCD Flat Panel Power Control: This signal is used enable power to the panel interface.
PANELBKLTEN	O CMOS	LVDS LCD Flat Panel Backlight Enable: This signal is used to enable the backlight inverter (BLI).
PANELBKLCTL	O CMOS	LVDS LCD Flat Panel Backlight Brightness Control: This signal is used as the Pulse Width Modulated (PWM) control signal to control the backlight inverter.
DDCCLK	I/O CMOS	CRT DDC Clock: This signal is used as the DDC clock signal between the CRT monitor and the GMCH.
DDCADATA	I/O CMOS	CRT DDC Data: This signal is used as the DDC data signal between the CRT monitor and the GMCH.
DDCPCLK	I/O CMOS	Panel DDC Clock: This signal is used as the DDC clock signal between the LFP and the GMCH.
DDCPADATA	I/O CMOS	Panel DDC Data: This signal is used as the DDC data signal between the LFP and the GMCH.
MI2CCLK	I/O DVO	DVO I2C Clock: This signal is used as the I2C_CLK for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MI2CDATA	I/O DVO	DVO I2C Data: This signal is used as the I2C_DATA for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MDVICLK	I/O DVO	DVI DDC Clock: This signal is used as the DDC clock for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDVIDATA	I/O DVO	DVI DDC Data: The signal is used as the DDC data for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDDCDATA	I/O DVO	DVI DDC Clock: The signal is used as the DDC data for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.
MDDCCLK	I/O DVO	DVI DDC Data: The signal is used as the DDC clock for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.

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5.2 Intel 82855GM Memory Controller Hub (Odem)

Voltage Reference, PLL Power Signals

Signal Name	Type	Description
Host Processor		
HXRCOMP	Analog	Host RCOMP: Used to calibrate the Host AGTL+ I/O buffers.
HYRCOMP	Analog	Host RCOMP: Used to calibrate the Host AGTL+ I/O buffers.
HXSWING	Analog	Host Voltage Swing (RCOMP reference voltage): These signals provide a reference voltage used by the PSB RCOMP circuit.
HYSWING	Analog	Host Voltage Swing (RCOMP reference voltage): These signals provide a reference voltage used by the PSB RCOMP circuit.
HADVREF[2:0]	Ref Analog	Host Data (input buffer) VREF: Reference voltage input for the data signals of the Host AGTL+ Interface. Input buffer differential amplifier to determine a high versus low input voltage.
HAVREF	Ref Analog	Host Address (input buffer) VREF: Reference voltage input for the address signals of the Host AGTL+ Interface. This signal is connected to the input buffer differential amplifier to determine a high versus low input voltage.
HCCVREF	Ref Analog	Host Common Clock (Command input buffer) VREF: Reference voltage input for the common clock signals of the Host AGTL+ Interface. This signal is connected to the input buffer differential amplifier to determine a high versus low input voltage.
VTTLF	Power	PSB Power Supply: VTTLF is the low frequency connection from the board. This signal is the primary connection of power for GMCH.
VTTHF	Power	PSB Power Supply: VTTHF is the high frequency supply. It is for direct connection from an internal package plane to a capacitor placed immediately adjacent to the GMCH. NOTE: Not to be connected to power rail.
System Memory		
SMRCOMP	Analog	System Memory RCOMP: This signal is used to calibrate the memory I/O buffers.
SMVREF_0	Ref Analog	Memory Reference Voltage(Input buffer VREF): Reference voltage input for Memory Interface. Input buffer differential amplifier to determine a high versus low input voltage.
SMVSWINGH	Ref Analog	RCOMP reference voltage: This is connected to the RCOMP buffer differential amplifier and is used to calibrate the I/O buffers.
SMVSWINGL	Ref Analog	RCOMP reference voltage: This is connected to the RCOMP buffer differential amplifier and is used to calibrate the I/O buffers.
VCCSM	Power	Power supply for Memory I/O.
VCCQSM	Power	Power supply for System Memory clock buffers.
VCCASM	Power	Power supply for System Memory logic running at the core voltage (isolated supply, not connected to the core).

Voltage Reference, PLL Power Signals Continue

Signal Name	Type	Description
Hub Interface		
HLRCOMP	Analog	Hub Interface RCOMP: This signal is connected to a reference resistor in order to calibrate the buffers.
PSWING	Ref Analog	Input buffer VREF: Input buffer differential amplifier to determine a high versus low input voltage.
VCCHL	Power	Power supply for Hub Interface buffers
DVO		
DVORCOMP	Analog	Compensation for DVO: This signal is used to calibrate the DVO I/O buffers.
GVREF	Ref Analog	Input buffer VREF: Input buffer differential amplifier to determine a high versus low input voltage.
VCCDVO	Power	Power supply for DVO.
GPIO		
VCCGPIO	Power	Power supply for GPIO buffers
DAC		
REFSET	Ref Analog	Resistor Set: Set point resistor for the internal color palette DAC.
VCCADAC	Power	Power supply for the DAC
VSSADAC	Power	Ground supply for the DAC
LVDS		
LIBG	Analog	LVDS reference current: signal connected to reference resistor.
VCCDLVDS	Power	Digital power supply.
VCCTXLVDS	Power	Data/Clock Tx power supply.
VCCALVDS	Power	Analog power supply.
VSSALVDS	Power	Ground supply for LVDS.
Clocks		
VCCAHPLL	Power	Power supply for the Host PLL.
VCCAGPLL	Power	Power supply for the Hub/DVO PLL.
VCCADPLLA	Power	Power supply for the display PLL A.
VCCADPLLB	Power	Power supply for the display PLL B.
Core		
VCC	Power	Power supply for the core.
VSS	Power	Ground supply for the chip.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Hub Interface Signals

Signal Name	Type	Description
HI[11:0]	I/O	Hub Interface Signals
HI_STB/HI_STBS	I/O	Hub Interface Strobe/ Hub Interface Strobe Second: One of two differential strobe signals used to transmit and receive data through the hub interface. Hub Interface 1.5 mode this signal is not differential and is the second of the two strobe signals.
HI_STB#/ HI_STBF	I/O	Hub Interface Strobe Complement / Hub Interface Strobe First: One of two differential strobe signals used to transmit and receive data through the hub interface. Hub Interface 1.5 mode this signal is not differential and is the first of the two strobe signals.
HICOMP	I/O	Hub Interface Compensation: Used for hub interface buffer compensation.
HI_VSWING	I	Hub Interface Voltage Swing: Analog input used to control the voltage swing and impedance strength of hub interface pins.

LAN Connect Interface Signals

Signal Name	Type	Description
LAN_CLK	I	LAN I/F Clock: Driven by the LAN Connect component. Frequency range is 5 MHz to 50 MHz.
LAN_RXD[2:0]	I	Received Data: The LAN Connect component uses these signals to transfer data and control information to the integrated LAN Controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	Transmit Data: The integrated LAN Controller uses these signals to transfer data and control information to the LAN Connect component.
LAN_RSTSYNC	O	LAN Reset/Sync: The LAN Connect component's Reset and Sync signals are multiplexed onto this pin.

EEPROM Interface Signals

Signal Name	Type	Description
EE_SHCLK	O	EEPROM Shift Clock: Serial shift clock output to the EEPROM.
EE_DIN	I	EEPROM Data In: Transfers data from the EEPROM to the ICH3. This signal has an integrated pull-up resistor.
EE_DOUT	O	EEPROM Data Out: Transfers data from the ICH3 to the EEPROM.
EE_CS	O	EEPROM Chip Select: Chip select signal to the EEPROM.

Firmware Hub Interface Signals

Signal Name	Type	Description
FWH[3:0]/ LAD[3:0]	I/O	Firmware Hub Signals. Muxed with LPC address signals.
FWH[4]/ LFRAME#	I/O	LFRAME# Firmware Hub Signals. Muxed with LPC LFRAME# signal.

PCI Interface Signals

Signal Name	Type	Description																								
AD[31:0]	I/O	PCI Address/Data: AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The ICH4 drives all 0s on AD[31:0] during the address phase of all PCI Special Cycles.																								
C/BE[3:0]#	I/O	Bus Command and Byte Enables: The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# define the Byte Enables. <table><tr><th>C/BE[3:0]#</th><th>Command Type</th></tr><tr><td>0 0 0 0</td><td>Interrupt Acknowledge</td></tr><tr><td>0 0 0 1</td><td>Special Cycle</td></tr><tr><td>0 0 1 0</td><td>I/O Read</td></tr><tr><td>0 0 1 1</td><td>I/O Write</td></tr><tr><td>0 1 1 0</td><td>Memory Read</td></tr><tr><td>0 1 1 1</td><td>Memory Write</td></tr><tr><td>1 0 1 0</td><td>Configuration Read</td></tr><tr><td>1 0 1 1</td><td>Configuration Write</td></tr><tr><td>1 1 0 0</td><td>Memory Read Multiple</td></tr><tr><td>1 1 1 0</td><td>Memory Read Line</td></tr><tr><td>1 1 1 1</td><td>Memory Write and Invalidate</td></tr></table> All command encodings not shown are reserved. The ICH4 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.	C/BE[3:0]#	Command Type	0 0 0 0	Interrupt Acknowledge	0 0 0 1	Special Cycle	0 0 1 0	I/O Read	0 0 1 1	I/O Write	0 1 1 0	Memory Read	0 1 1 1	Memory Write	1 0 1 0	Configuration Read	1 0 1 1	Configuration Write	1 1 0 0	Memory Read Multiple	1 1 1 0	Memory Read Line	1 1 1 1	Memory Write and Invalidate
C/BE[3:0]#	Command Type																									
0 0 0 0	Interrupt Acknowledge																									
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0 0 1 0	I/O Read																									
0 0 1 1	I/O Write																									
0 1 1 0	Memory Read																									
0 1 1 1	Memory Write																									
1 0 1 0	Configuration Read																									
1 0 1 1	Configuration Write																									
1 1 0 0	Memory Read Multiple																									
1 1 1 0	Memory Read Line																									
1 1 1 1	Memory Write and Invalidate																									
DEVSEL#	I/O	Device Select: The ICH4 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH4 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH4 address or an address destined for the hub interface (main memory or AGP). As an input, DEVSEL# indicates the response to an ICH4-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated by the ICH4 until driven by a Target device.																								

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

PCI Interface Signals (Continued)

Signal Name	Type	Description
FRAME#	I/O	Cycle Frame: The current Initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the Initiator asserts FRAME#, data transfers continue. When the Initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH4 when the ICH4 is the Target, and FRAME# is an output from the ICH4 when the ICH4 is the Initiator. FRAME# remains tri-stated by the ICH4 until driven by an Initiator.
IRDY#	I/O	Initiator Ready: IRDY# indicates the ICH4's ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock that both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH4 has valid data present on AD[31:0]. During a read, it indicates the ICH4 is prepared to latch data. IRDY# is an input to the ICH4 when the ICH4 is the Target and an output from the ICH4 when the ICH4 is an Initiator. IRDY# remains tri-stated by the ICH4 until driven by an Initiator.
TRDY#	I/O	Target Ready: TRDY# indicates the ICH4's ability, as a Target, to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH4, as a Target, has placed valid data on AD[31:0]. During a write, TRDY# indicates that the ICH4, as a Target, is prepared to latch data. TRDY# is an input to the ICH4 when the ICH4 is the Initiator and an output from the ICH4 when the ICH4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated by the ICH4 until driven by a target.
PAR	I/O	Calculated/Checked Parity: PAR uses "even" parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. "Even" parity means that the ICH4 counts the number of 1s within the 36 bits plus PAR and the sum is always even. The ICH4 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH4 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH4 drives and tri-states PAR identically to the AD[31:0] lines except that the ICH4 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH4 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. ICH4 checks parity when it is the Target of a PCI write transaction. If a parity error is detected, the ICH4 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.

PCI Interface Signals (Continued)

Signal Name	Type	Description
STOP#	I/O	Stop: STOP# indicates that the ICH4, as a Target, is requesting the Initiator to stop the current transaction. STOP# causes the ICH4, as an Initiator, to stop the current transaction. STOP# is an output when the ICH4 is a Target and an input when the ICH4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by the ICH4.
PERR#	I/O	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error. The ICH4 drives PERR# when it detects a parity error. The ICH4 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ[4:0]# REQ[5]# / REQ[B]# / GPIO[1]	I	PCI Requests: The ICH4 supports up to 6 masters on the PCI bus. REQ[5]# is muxed with PC/PCI REQ[B]# (must choose one or the other, but not both). If not used for PCI or PC/PCI, REQ[5]#/REQ[B]# can instead be used as GPIO[1]. NOTE: REQ[0]# is programmable to have improved arbitration latency for supporting PCI-based 1394 controllers.
GNT[4:0]# GNT[5]# / GNT[B]# / GPIO[17]	O	PCI Grants: The ICH4 supports up to 6 masters on the PCI bus. GNT[5]# is muxed with PC/PCI GNT[B]# (must choose one or the other, but not both). If not needed for PCI or PC/PCI, GNT[5]# can instead be used as a GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. GNT[B]#/GNT[5]#/GPIO[17] has an internal pull-up.
PCICLK	I	PCI Clock: This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus. NOTE: This clock does not stop based on STP_PCI# signal. PCICLK only stops based on SLP_S1# or SLP_S3#.
PCIRST#	O	PCI Reset: ICH4 asserts PCIRST# to reset devices that reside on the PCI bus. The ICH4 asserts PCIRST# during power-up and when S/W initiates a hard reset sequence through the RC (CF9h) register. The ICH4 drives PCIRST# inactive a minimum of 1 ms after PWROK is driven active. The ICH4 drives PCIRST# active a minimum of 1 ms when initiated through the RC register.
PLOCK#	I/O	PCI Lock: This signal indicates an exclusive bus operation and may require multiple transactions to complete. ICH4 asserts PLOCK# when it performs non-exclusive transactions on the PCI bus. Devices on the PCI bus (other than the ICH4) are not permitted to assert the PLOCK# signal.
SERR#	I/OD	System Error: SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH4 has the ability to generate an NMI, SMI#, or interrupt.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

PCI Interface Signals (Continued)

Signal Name	Type	Description
PME#	I/OD	PCI Power Management Event: PCI peripherals drive PME# to wake the system from low-power states S1-M-S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH4 may drive PME# active due to an internal wake event. The ICH4 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.
CLKRUN#	I/O	PCI Clock Run: Used to support PCI Clock Run protocol. Connects to PCI devices that need to request clock re-start, or prevention of clock stopping. NOTE: An external pull-up to the core power plane is required.
REQ[A]#/ GPIO[0] REQ[B]#/ REQ[5]#/ GPIO[1]	I	PC/PCI DMA Request [A:B]: This request serializes ISA-like DMA Requests for the purpose of running ISA-compatible DMA cycles over the PCI bus. This is used by devices such as PCI based Super I/O or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI requests, these signals can be used as General Purpose Inputs. REQ[B]# can instead be used as the 6th PCI bus request.
GNT[A]#/ GPIO[16] GNT[B]#/ GNT[5]#/ GPIO[17]	O	PC/PCI DMA Acknowledges [A: B]: This grant serializes an ISA-like DACK# for the purpose of running DMA/ISA Master cycles over the PCI bus. This is used by devices such as PCI based Super I/O or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI, these signals can be used as General Purpose Outputs. GNTB# can also be used as the 6th PCI bus master grant output. These signal have internal pull-up resistors.

IDE Interface Signals

Signal Name	Type	Description
PDCS1#, SDCS1#	O	Primary and Secondary IDE Device Chip Selects for 100 Range: For ATA command register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDCS3#, SDCS3#	O	Primary and Secondary IDE Device Chip Select for 300 Range: For ATA control register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDA[2:0], SDA[2:0]	O	Primary and Secondary IDE Device Address: These output signals are connected to the corresponding signals on the primary or secondary IDE connectors. They are used to indicate which byte in either the ATA command block or control block is being addressed.

IDE Interface Signals Continue

Signal Name	Type	Description
PDD[15:0], SDD[15:0]	I/O	Primary and Secondary IDE Device Data: These signals directly drive the corresponding signals on the primary or secondary IDE connector. There is a weak internal pull-down resistor on PDD[7] and SDD[7].
PDDREQ, SDDREQ	I	Primary and Secondary IDE Device DMA Request: These input signals are directly driven from the DRQ signals on the primary or secondary IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function and are not associated with any AT compatible DMA channel. There is a weak internal pull-down resistor on these signals.
PDDACK#, SDDACK#	O	Primary and Secondary IDE Device DMA Acknowledge: These signals directly drive the DAK# signals on the primary and secondary IDE connectors. Each is asserted by the ICH4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
PDIOR#/ (PDWSTB/PRDMA RDY#) SDIOR#/ (SDWSTB/SRDMA RDY#)	O	Primary and Secondary Disk I/O Read (PIO and Non-Ultra DMA): This is the command to the IDE device that it may drive data onto the PDD or SDD lines. Data is latched by the ICH4 on the deassertion edge of PDIOR# or SDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDSCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). Primary and Secondary Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, ICH4 drives valid data on rising and falling edges of PDWSTB or SDWSTB. Primary and Secondary Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, ICH4 deasserts PRDMARDY# or SRDMARDY# to pause burst data transfers.
PDIOW#/ (PDSTOP) SDIOW#/ (SDSTOP)	O	Primary and Secondary Disk I/O Write (PIO and Non-Ultra DMA): This is the command to the IDE device that it may latch data from the PDD or SDD lines. Data is latched by the IDE device on the deassertion edge of PDIOW# or SDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDSCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). Primary and Secondary Disk Stop (Ultra DMA): ICH4 asserts this signal to terminate a burst.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

IDE Interface Signals (Continued)

Signal Name	Type	Description
PIORDY# /(PDRSTB/PWDMA RDY#)	I	Primary and Secondary I/O Channel Ready (PIO): This signal will keep the strobe active (PDIOR# or SDIOR# on reads, PDIO# or SDIO# on writes) longer than the minimum width. It adds wait states to PIO transfers. Primary and Secondary Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, the ICH4 latches data on rising and falling edges of this signal from the disk. Primary and Secondary Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is de-asserted by the disk to pause burst data transfers.
SIORDY# /(SDRSTB/SWDMA RDY#)		

Interrupt Signals

Signal Name	Type	Description
SERIRQ	I/O	Serial Interrupt Request: This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	PCI Interrupt Requests: In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]# /GPIO[5:2]	I/OD	PCI Interrupt Requests: In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.
IRQ[14:15]	I	Interrupt Request 14:15: These interrupt inputs are connected to the IDE drives. IRQ14 is used by the drives connected to the Primary controller and IRQ15 is used by the drives connected to the Secondary controller.
APICCLK	I	APIC Clock: This clock operates up to 33.33 MHz.
APICD[1:0]	I/OD	APIC Data: These bi-directional open drain signals are used to send and receive data over the APIC bus. As inputs the data is valid on the rising edge of APICCLK. As outputs, new data is driven from the rising edge of the APICCLK.

LPC Interface Signals

Signal Name	Type	Description
LAD[3:0]/FWH[3:0]	I/O	LPC Multiplexed Command, Address, Data: For the LAD[3:0] signals, internal pull-ups are provided.
LFRAME# /FWH[4]	O	LPC Frame: LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ[1:0]#	I	LPC Serial DMA/Master Request Inputs: LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to an external Super I/O device. An internal pull-up resistor is provided on these signals.

USB Interface Signals

Signal Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	Universal Serial Bus Port 1:0 Differential: These differential pairs are used to transmit data/address/command signals for ports 0 and 1. These ports can be routed to USB UHCI Controller #1 or the USB EHCI Controller. NOTE: No external resistors are required on these signals. The ICH4 integrates 15 k Ω pull-downs and provides an output driver impedance of 45 Ω , which requires no external series resistor.
USBP2P, USBP2N, USBP3P, USBP3N	I/O	Universal Serial Bus Port 3:2 Differential: These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to USB UHCI Controller #2 or the USB EHCI Controller. NOTE: No external resistors are required on these signals. The ICH4 integrates 15 k Ω pull-downs and provides an output driver impedance of 45 Ω , which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP4N	I/O	Universal Serial Bus Port 5:4 Differential: These differential pairs are used to transmit data/address/command signals for ports 4 and 5. These ports can be routed to USB UHCI Controller #3 or the USB EHCI Controller. NOTE: No external resistors are required on these signals. The ICH4 integrates 15 k Ω pull-downs and provides an output driver impedance of 45 Ω , which requires no external series resistor.
OC[5:0]#	I/O	Overcurrent Indicators: These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred.
USBRBIAS	O	USB Resistor Bias: Analog connection point for an external resistor to ground. USBRBIAS should be connected to USBRBIAS# as close to the resistor as possible.
USBRBIAS#	I	USB Resistor Bias Complement: Analog connection point for an external resistor to ground. USBRBIAS# should be connected to USBRBIAS as close to the resistor as possible.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Power Management Interface Signals

Signal Name	Type	Description
THRM#	I	Thermal Alarm: This is an active low signal generated by external hardware to start the hardware clock throttling mode. The signal can also generate an SMI# or an SCI.
THRMTRIP#	I	Thermal Trip: When low, THRMTRIP# indicates that a thermal trip from the processor occurred; the ICH4 will immediately transition to a S5 state. The ICH4 will not wait for the processor stop grant cycle since the processor has overheated.
SLP_S1#	O	S1 Sleep Control: SLP_S1# provides Clock Synthesizer or Power plane control. Optional use is to shut off power to non-critical systems when in the S1- M (Powered On Suspend), S3 (Suspend To RAM), S4 (Suspend to Disk) or S5 (Soft Off) states.
SLP_S3#	O	S3 Sleep Control: SLP_S3# is for power plane control. It shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	S4 Sleep Control: SLP_S4# is for power plane control. It shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state.
SLP_S5#	O	S5 Sleep Control: SLP_S5# is for power plane control. The signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
PWROK	I	Power OK: When asserted, PWROK is an indication to the ICH4 that core power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, the ICH4 asserts PCIRST#. NOTE: PWROK must deassert for a minimum of 3 RTC clock periods for the ICH4 to fully reset the power and properly generate the PCIRST# output
PWRBTN#	I	Power Button: The Power Button causes SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal causes a wake event. If PWRBTN# is pressed for more than 4 seconds, this causes an unconditional transition (power button override) to the S5 state with only the PWRBTN# available as a wake event. Override occurs even if the system is in the S1-M-S4 states. This signal has an internal pull-up resistor.
RI#	I	Ring Indicate: This signal is an input from the modem interface. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	System Reset: This pin forces an internal reset after being debounced. The ICH4 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms $\pm$ 2 ms for the SMBus to idle before forcing a reset on the system.
RSMRST#	I	Resume Well Reset: This signal is used for resetting the resume power plane logic.

Power Management Interface Signals Continue

Signal Name	Type	Description
LAN_RST#	I	LAN Reset: This signal must be asserted at least 10 ms after the resume well power (VccLAN3_3 and VccLAN1_5 is valid. When deasserted, this signal is an indication that the resume well power is stable.
SUS_STAT#/LPCPD#	O	Suspend Status: This signal is asserted by the ICH4 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC I/F.
C3_STAT#	O	C3_STAT#: This signal will typically be configured as C3_STAT#. It is used for indicating to an AGP device that a C3 state transition is beginning or ending. If C3_STAT# functionality is not required, this signal may be used as a GPO. NOTE: This signal will be asserted in S1-M on the ICH4-M.
SUSCLK	O	Suspend Clock: Output of the RTC generator circuit to use by other chips for refresh clock.
AGPBUSY#	I	AGP Bus Busy: To support the C3 state. This signal is an indication that the AGP device is busy. When this signal is asserted, the BM_STS bit will be set. If this functionality is not needed, this signal may be configured as a GPI.
STP_PCI#	O	Stop PCI Clock: This signal is an output to the external clock generator for it to turn off the PCI clock. Used to support PCI CLKRUN# protocol. If this functionality is not needed, This signal can be configured as a GPO.
STP_CPU#	O	Stop CPU Clock: Output to the external clock generator for it to turn off the processor clock. Used to support the C3 state. If this functionality is not needed, this signal can be configured as a GPO.
BATLOW#	I	Battery Low: This signal is an input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S1-M-S5 state. Can also be enabled to cause an SMI# when asserted.
CPUPERF#	OD	CPU Performance: CPUPERF# is used for Intel SpeedStep technology support. The signal selects which power state to put the processor in.
SSMUXSEL	O	SpeedStep Mux Select: SSMUXSEL is used for Intel SpeedStep technology support. The signal selects the voltage level for the processor.
VGATE/VRMPWRGD	I	VGATE/VRM Power Good: VGATE/VRMPWRGD is used for Intel SpeedStep technology support. This is an output from the processor's voltage regulator to indicate that the voltage is stable. This signal may go inactive during an Intel SpeedStep transition.

8060B N/B Maintenance

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Power Management Interface Signals (Continued)

Signal Name	Type	Description
DPRSLPVR	O	Deeper Sleep - Voltage Regulator: This signal is used to lower the voltage of VRM during C4 and S1-M states. When the signal is high, the voltage regulator outputs the lower “Deeper Sleep” voltage. When the signal is low (default), the voltage regulator outputs the higher “Normal” voltage. During PCIRST#, the output driver is disabled and an internal pull-down is enabled. This is needed for implementing a strap on the pin. When PCIRST# deasserts, the output driver is enabled. To guarantee no glitches on the DPRSLPVR pin, the pull-down is disabled after the output driver is fully enabled. NOTE: DPRSLPVR is sampled at the rising edge of PWROK as a functional strap.

Processor Interface Signals

Signal Name	Type	Description
A20M#	O	Mask A20: A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active. Speed Strap: During the reset sequence, ICH4 drives A20M# high if the corresponding bit is set in the FREQ_STRP register.
CPUSLP#	O	CPU Sleep: This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The ICH4 can optionally assert the CPUSLP# signal when going to the S1-M state.
FERR#	I	Numeric Coprocessor Error: This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH4 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is asserted, the ICH4 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. NOTE: FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the General Control Register bit setting.
INTR	O	CPU Interrupt: INTR is asserted by the ICH4 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low. Speed Strap: During the reset sequence, ICH4 drives INTR high if the corresponding bit is set in the FREQ_STRP register.

Processor Interface Signals Continue

Signal Name	Type	Description
IGNNE#	O	Ignore Numeric Error: This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH4 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. Speed Strap: During the reset sequence, ICH4 drives IGNNE# high if the corresponding bit is set in the FREQ_STRP register.
INIT#	O	Initialization: INIT# is asserted by the ICH4 for 16 PCI clocks to reset the processor. ICH4 can be configured to support CPU BIST. In that case, INIT# will be active when PCIRST# is active.
NMI	O	Non-Maskable Interrupt: NMI is used to force a non-Maskable interrupt to the processor. The ICH4 can generate an NMI when either SERR# or IOCHK# is asserted. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. Speed Strap: During the reset sequence, ICH4 drives NMI high if the corresponding bit is set in the FREQ_STRP register.
SMI#	O	System Management Interrupt: SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH4 in response to one of many enabled hardware or software events.
STPCLK#	O	Stop Clock Request: STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH4 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	Keyboard Controller Reset CPU: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH4's other sources of INIT#. When the ICH4 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. NOTE: The ICH4 ignores RCIN# assertion during transitions to the S1-M, S3, S4 and S5 states.
A20GATE	I	A20 Gate: A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other PCIsets.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Processor Interface Signals (Continued)

Signal Name	Type	Description
CPUPWRGD	OD	CPU Power Good: This signal should be connected to the processor's PWRGOOD input. To allow for Intel® SpeedStep™ technology support, this signal is kept high during an Intel SpeedStep technology state transition to prevent loss of processor context. This is an open-drain output signal (external pull-up resistor required) that represents a logical AND of the ICH4's PWROK and VGATE / VRMPWRGD signals.
DPSLP#	O	Deeper Sleep: This signal is asserted by the ICH4 to the processor. When the signal is low, the processor enters the Deeper Sleep state by gating off the processor Core clock inside the processor. When the signal is high (default), the processor is not in the Deeper Sleep state. This signal behaves identically to the STP_CPU# signal, but at the processor voltage level.

SMBus Interface Signals

Signal Name	Type	Description
SMBDATA	I/OD	SMBus Data: External pull-up is required.
SMBCLK	I/OD	SMBus Clock: External pull-up is required.
SMBALERT#/GPIO[11]	I	SMBus Alert: This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPI.

System Management Interface Signals

Signal Name	Type	Description
INTRUDER#	I	Intruder Detect: Can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	System Management Link: SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK[0] corresponds to an SMBus Clock signal, and SMLINK[1] corresponds to an SMBus Data signal.

Real Time Clock Interface Signals

Signal Name	Type	Description
RTCX1	Special	Crystal Input 1: This signal is connected to the 32.768 kHz crystal.
RTCX2	Special	Crystal Input 2: This signal is connected to the 32.768 kHz crystal.

Other Clock Signals

Signal Name	Type	Description
CLK14	I	Oscillator Clock: Used for 8254 timers. It runs at 14.31818 MHz. This clock is permitted to stop during S1-M (or lower) states.
CLK48	I	48 MHz Clock: This clock is used to run the USB controller. It runs at 48 MHz. This clock is permitted to stop during S1-M (or lower) states.
CLK66	I	66 MHz Clock: This is used to run the hub interface. It runs at 66 MHz. This clock is permitted to stop during S1-M (or lower) states.

Miscellaneous Signals

Signal Name	Type	Description
SPKR	O	Speaker: The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PCIRST#, its output state is 0. NOTE: SPKR is sampled at the rising edge of PWROK as a functional strap.
RTCST#	I	RTC Reset: When asserted, this signal resets register bits in the RTC well and sets the RTC_PWR_STS bit (bit 2 in GEN_PMCN3 register). NOTES: 1. Clearing CMOS in an ICH4-based platform can be done by using a jumper on RTCST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. 2. Unless entering the XOR Chain Test Mode, the RTCST# input must always be high when all other RTC power planes are on.

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5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

AC'97 Link Signals

Signal Name	Type	Description
AC_RST#	O	AC '97 Reset: This signal is a master hardware reset to external Codec(s).
AC_SYNC	O	AC '97 Sync: This signal is a 48 kHz fixed rate sample sync to the Codec(s).
AC_BIT_CLK	I	AC97 Bit Clock: This signal is a 12.288 MHz serial data clock generated by the external Codec(s). This signal has an integrated pull-down resistor.
AC_SDOUT	O	AC97 Serial Data Out: Serial TDM data output to the Codec(s). NOTE: AC_SDOUT is sampled at the rising edge of PWROK as a functional strap.
AC_SDIN[1:0]	I	AC97 Serial Data In 2:0: These signals are Serial TDM data inputs from the three Codecs.

NOTE: An integrated pull-down resistor on AC_BIT_CLK is enabled when either: The ACLINK Shutoff bit in the AC'97 Global Control Register is set to 1, or Both Function 5 and Function 6 of Device 31 are disabled. Otherwise, the integrated pull-down resistor is disabled.

General Purpose I/O Signals

Signal Name	Type	Description
GPIO[43:32]	I/O	Can be input or output. Main power well.
GPIO[31:29]	O	Not implemented.
GPIO[28:27]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[26]	I/O	Not implemented.
GPIO[25]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[24:18]	I/O	Not Implemented in Mobile (Assign to native Functionality).
GPIO[17:16]	O	Fixed as Output only. Main power well. Can be used instead as PC/PCI GNT[A:B]#. GPIO[17] can also alternatively be used for PCI GNT[5]#. Integrated pull-up resistor.
GPIO[15:14]	I	Not implemented.
GPIO[13:12]	I	Fixed as Input only. Resume power well. Unmuxed.
GPIO[11]	I	Fixed as Input only. Resume power well. Can be used instead as SMBALERT#.
GPIO[10:9]	I	Not implemented.
GPIO[8]	I	Fixed as Input only. Resume power well. Unmuxed.
GPIO[7]	I	Fixed as Input only. Main power well. Unmuxed.
GPIO[6]	I	Not Implemented in Mobile (Assign to Native Functionality)
GPIO[5:2]	I	Fixed as Input only. Main power well. Can be used instead as PIRQ[E:H]#.
GPIO[1:0]	I	Fixed as Input only. Main power well. Can be used instead as PC/PCI REQ[A:B]#. GPIO[1] can also alternatively be used for PCI REQ[5]#.

NOTE: Main power well GPIO are 5V tolerant, except for GPIO[43:32]. Resume power well GPIO are not 5V tolerant.

Power and Ground Signals

Signal Name	Description
VCC3_3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VCC1_5	1.5 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
VCCHI	1.5 V supply for Hub Interface 1.5 logic. 1.8 V supply for Hub Interface 1.0 logic. This power may be shut off in S3, S4, S5 or G3 states.
V5REF	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
HIREF	Analog Input. Expected voltages are: • 0.9 V for HI 1.0 (Normal Hub Interface) Series Termination • 350 mV for HI 1.5 (Enhanced Hub Interface) Parallel Termination This power is shut off in S3, S4, S5, and G3 states.
VCCSUS3_3	3.3 V supply for resume well I/O buffers. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
VCCSUS1_5	1.5 V supply for resume well logic. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
V5REF_SUS	Reference for 5 V tolerance on resume well inputs. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
VCCLAN3_3	3.3 V supply for LAN Connect interface buffers. This is a separate power plane that may or may not be powered in S3–S5 states depending upon the presence or absence of AC power and network connectivity. This plane must be on in S0 and S1-M.
VCCLAN1_5	1.5 V supply for LAN Controller logic. This is a separate power plane that may or may not be powered in S3–S5 states depending upon the presence or absence of AC power and network connectivity. This plane must be on in S0 and S1-M.
VCCRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. NOTE: Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an ICH4-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap.
VCCPLL	1.5 V supply for core well logic. This signal is used for the USB PLL. This power may be shut off in S3, S4, S5 or G3 states.
VBIAS	RTC well bias voltage. The DC reference voltage applied to this pin sets a current that is mirrored throughout the oscillator and buffer circuitry.
V_CPU_IO	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface outputs.
VSS	Grounds.

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7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at PIO Port or Mini PCI Slot.

8060B N/B Maintenance

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
00h	Boot started
01h	Disable A20 through A20
02h	Initialize chipset
03h	Test RAM
04h	Move BL into the RAM
05h	Execution in RAM
06h	User Flash Check
07h	Shadow system BIOS
08h	Checksum System BIOS ROM
09h	Proceed with Normal Boot
0Ah	Proceed with Crisis Boot
0Bh	Initialize Clock Sythesizer
0Fh	Fatal Error
10h	Some Type of Long Reset
11h	Turn Off Fasta20 for Post
12h	Signal Power On Reset

Code	POST Routine Description
13h	Initialize the Chipset
14h	Search For ISA Bus VGA Adapter
15h	Reset Counter/Timer 1
16h	User Register Config Through CMOS
17h	Size Memory
18h	Dispatch to RAM Test
19h	Checksum the ROM
1Ah	Reset PIC's
1Bh	Initialize Video Adapter
1Ch	Initialize Video(6845 Regs)
1Dh	Initialize Color Adapter
1Eh	Initialize Monochrome Adapter
1Fh	Test 8237A Page Registers
20h	Test Keyboard
21h	Test Keyboard Controller
22h	Check If CMOS Ram Valid

8060B N/B Maintenance

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
23h	Test Battery Fail & CMOS X-SUM
24h	Test DMA Controller
25h	Initialize 8237A Controller
26h	Initialize Int Vectors
27h	RAM Quick Sizing
28h	Protected mode entered safely
29h	RAM Test Completed
2Ah	Protected mode exit successful
2Bh	Setup Shadow
2Ch	Going to Initialize Video
2Dh	Search For Monochrome Adapter
2Eh	Search For Color Adapter
2Fh	Signal Messages Displayed
30h	Special Into of Keyboard Controller
31h	Test If Keyboard Present
32h	Test Keyboard Interrupt

Code	POST Routine Description
33h	Test Keyboard Command Byte
34h	TEST, Blank and Count All RAM
35h	Protected mode entered safely
36h	RAM Test Complete
37h	Protected mode exit successful
38h	Update Output Port
39h	Setup Cache Controller
3Ah	Test If 18.2Hz Periodic Working
3Bh	Test for RTC ticking
3Ch	Initialize the Hardware Vectors
3Dh	Search and Init the Mouse
3Eh	Update NumLock Status
3Fh	Special init of COMM and LPT ports
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the Hard Disk

8060B N/B Maintenance

7.2 Error Codes

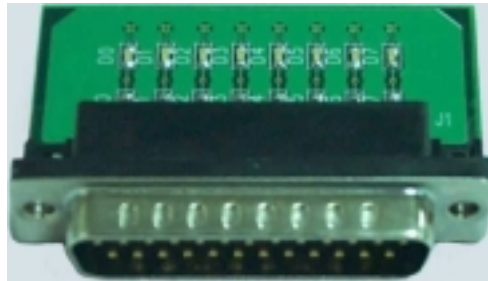
Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NumLock Status
46h	Test For Coprocessor Installed
47h	OEM Function Before Boot
48h	Dispatch To Op.Sys.Boot
49h	Jump Into Bootstrap Code
99h	Resume SMRAM not Found

8060B N/B Maintenance

7.3 Maintenance Diagnostics

7.3.1 Diagnostic Tool for PIO Port :

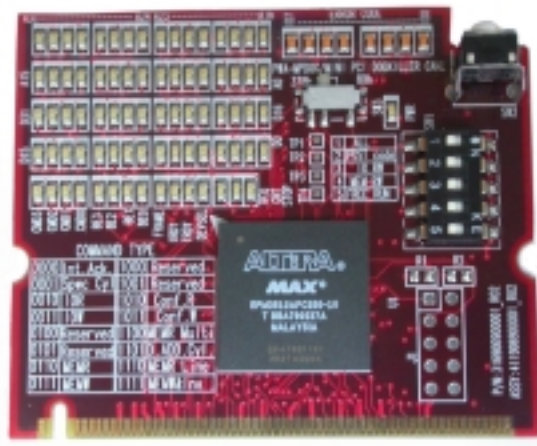


P/N:411904800001

Description: PWA; PWA-378 Port Debug BD

Note: Order it from MIC/TSSC

7.3.2 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001

Description: PWA; PWA-378 Port Debug BD

Note: Order it from MIC/TSSC

8060B N/B Maintenance

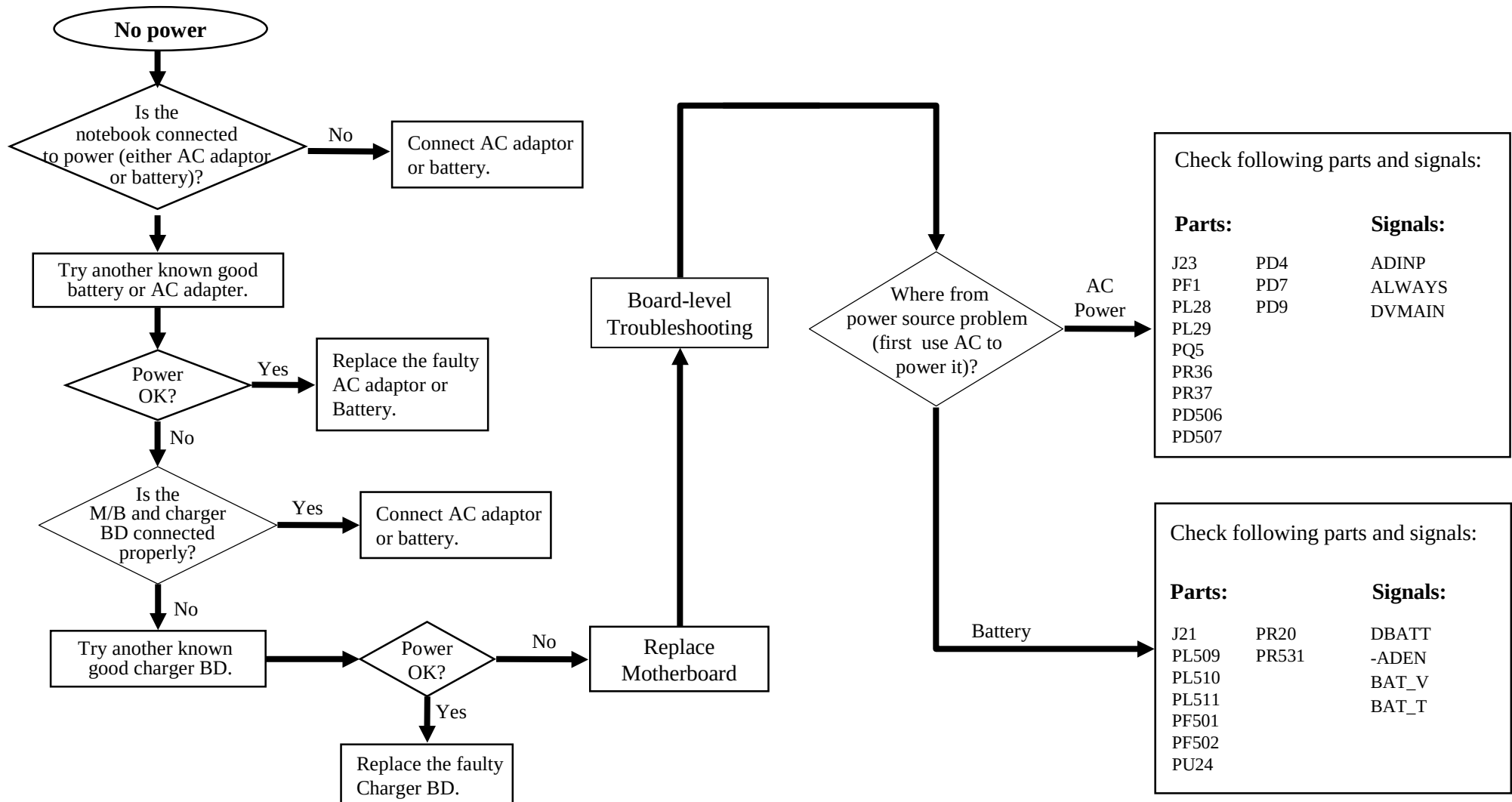
8. Trouble Shooting

- ☐ **8.1 No Power**
- ☐ **8.2 No Display**
- ☐ **8.3 VGA Controller Failure LCD No Display**
- ☐ **8.4 External Monitor No Display**
- ☐ **8.5 Memory Test Error**
- ☐ **8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error**
- ☐ **8.7 Hard Driver Test Error**
- ☐ **8.8 CD-ROM Driver Test Error**
- ☐ **8.9 PIO Port Test Error**
- ☐ **8.10 USB Port Test Error**
- ☐ **8.11 Audio Failure**
- ☐ **8.12 LAN Test Error**
- ☐ **8.13 PC Card Socket and IEEE1394 Failure**

8060B N/B Maintenance

8.1 No Power

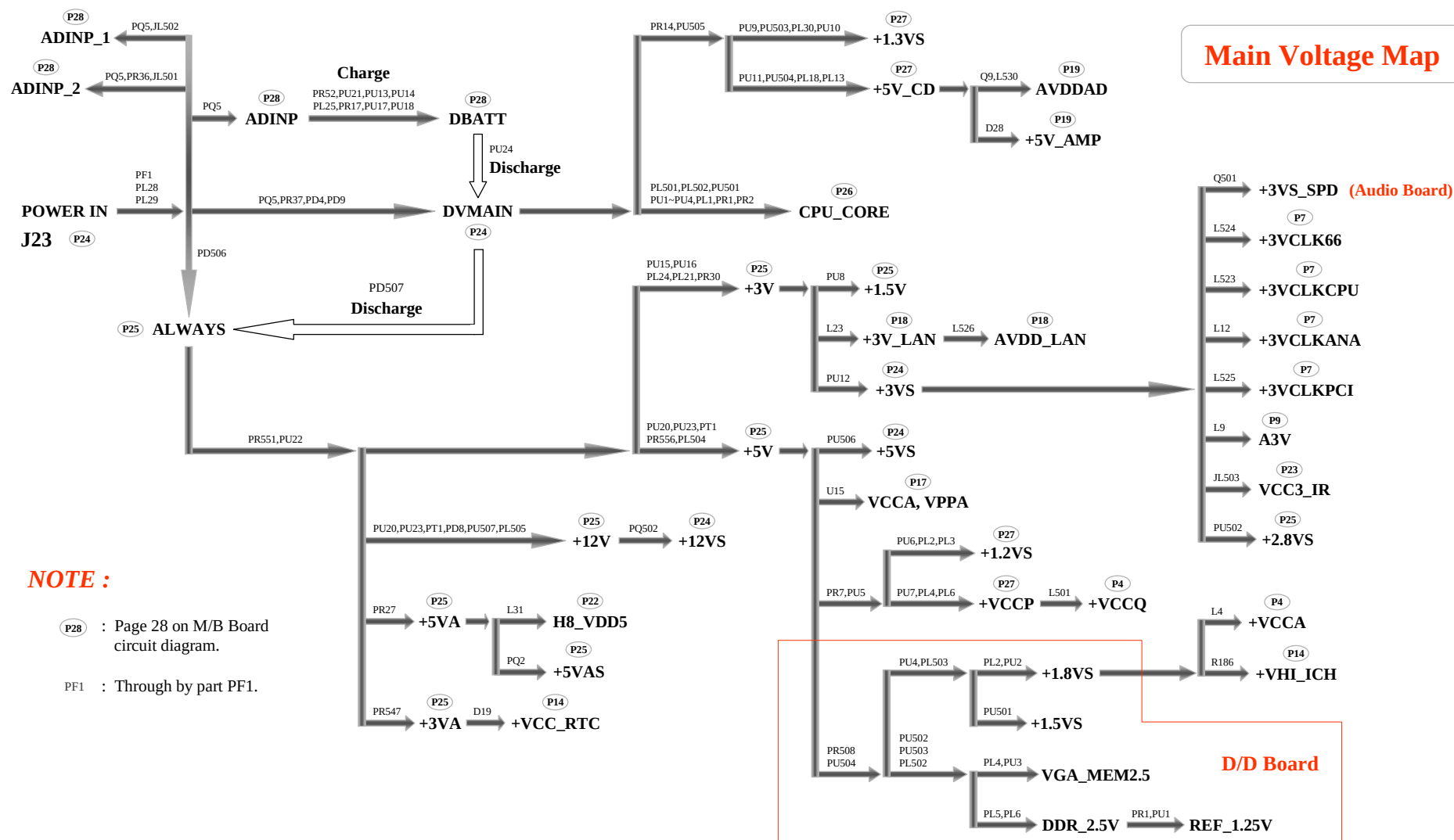
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8060B N/B Maintenance

8.1 No Power

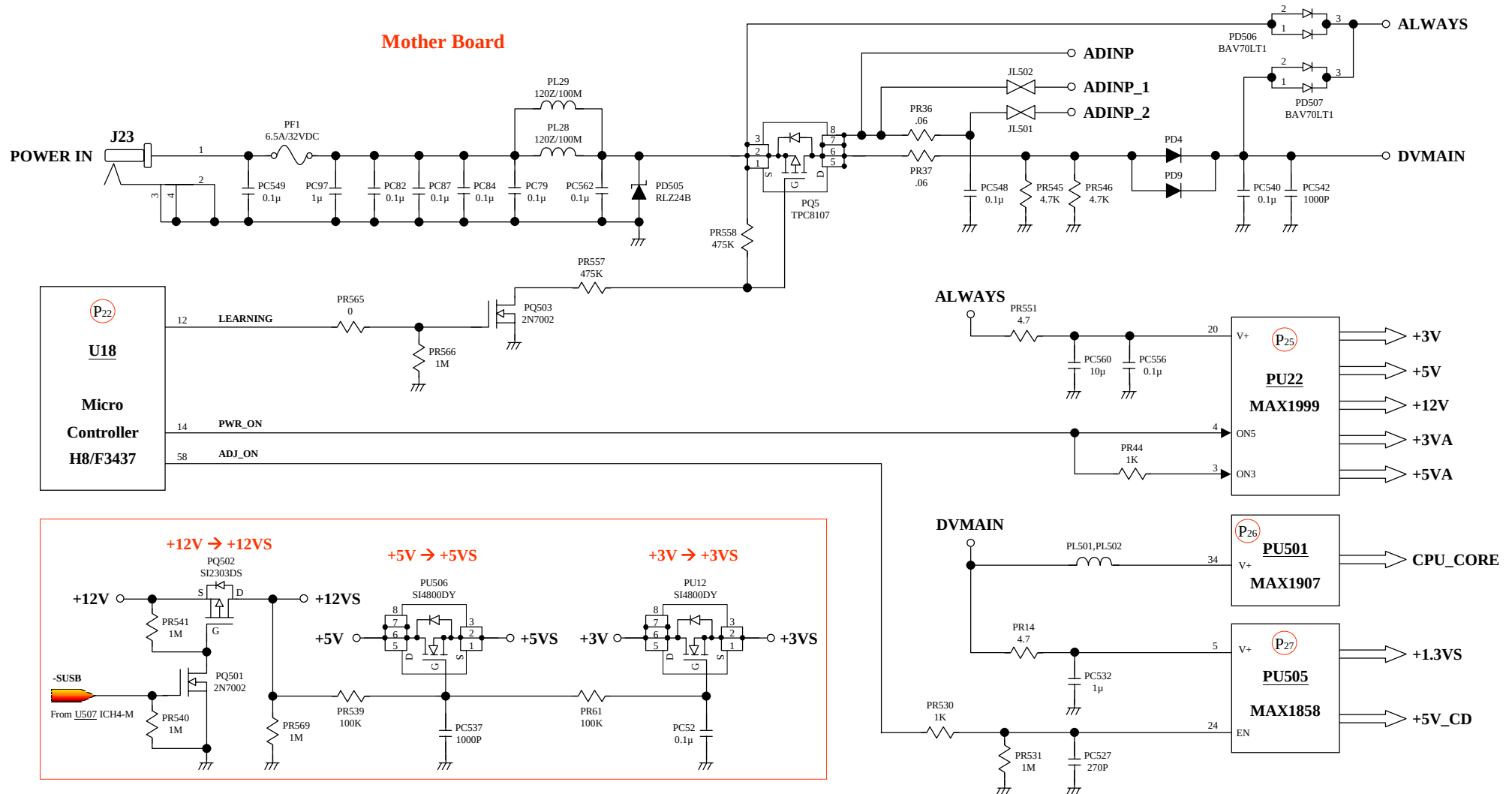
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8060B N/B Maintenance

8.1 No Power

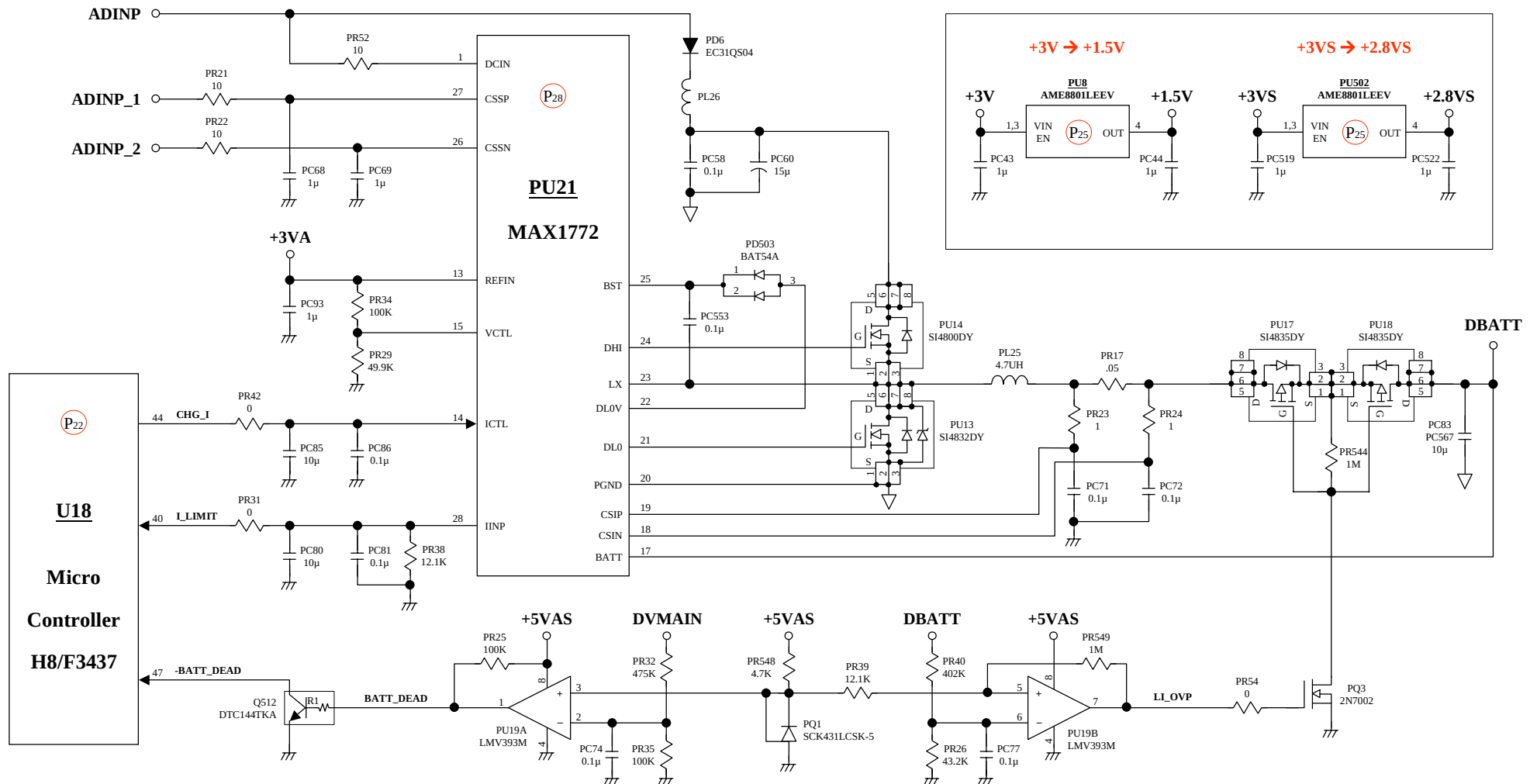
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8060B N/B Maintenance

8.1 No Power

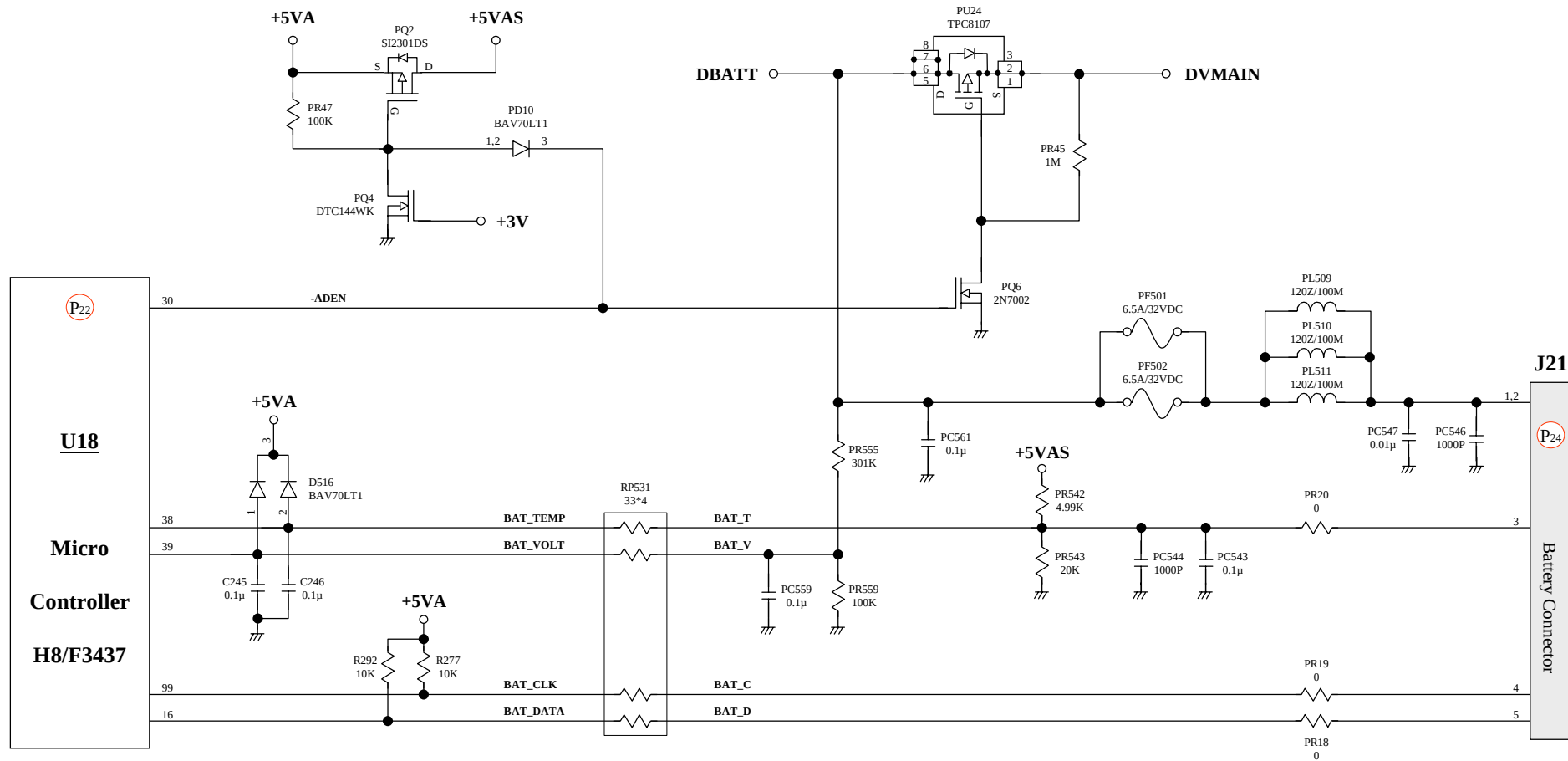
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8060B N/B Maintenance

8.1 No Power

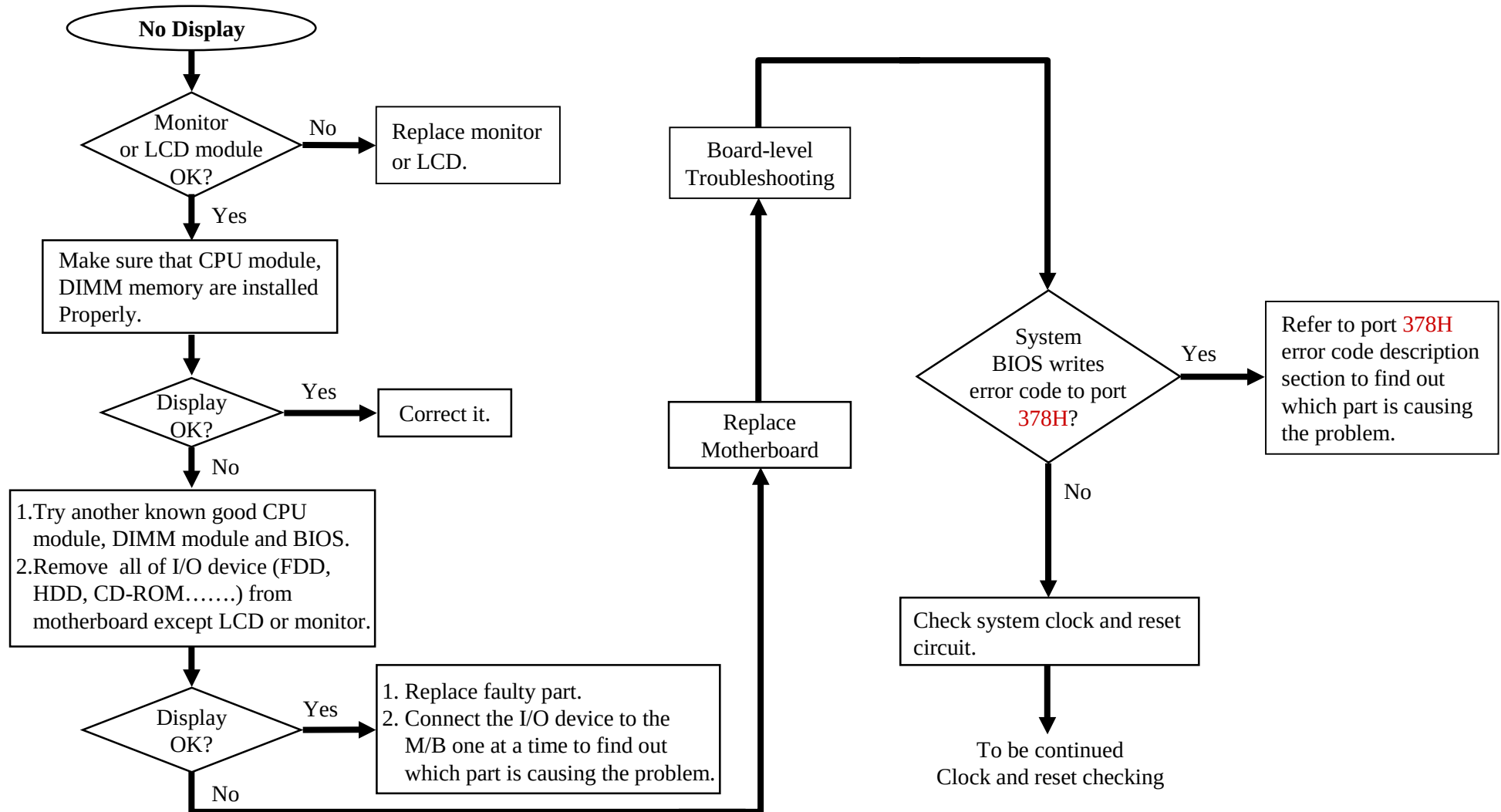
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8060B N/B Maintenance

8.2 No Display

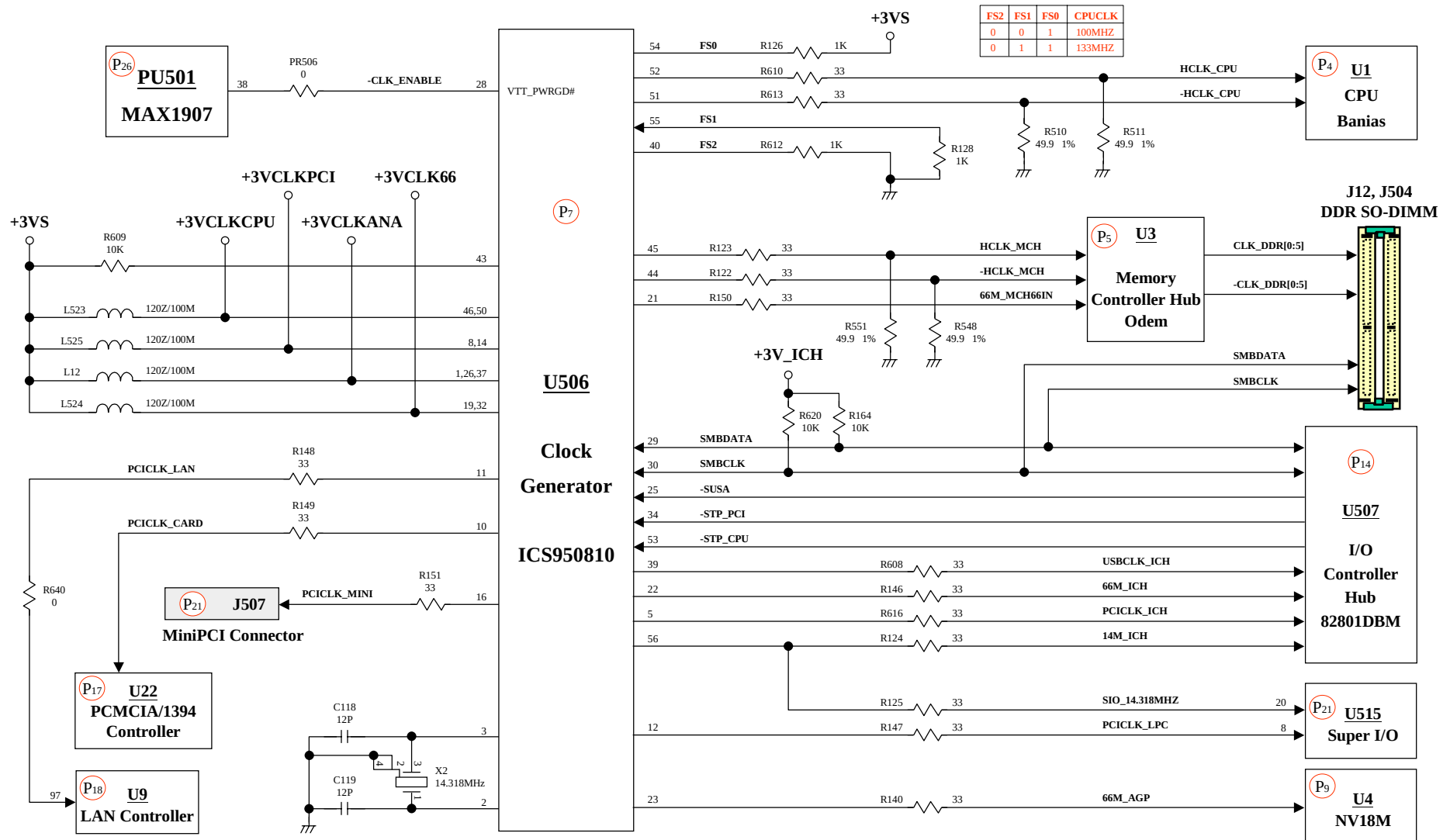
There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



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8.2 No Display

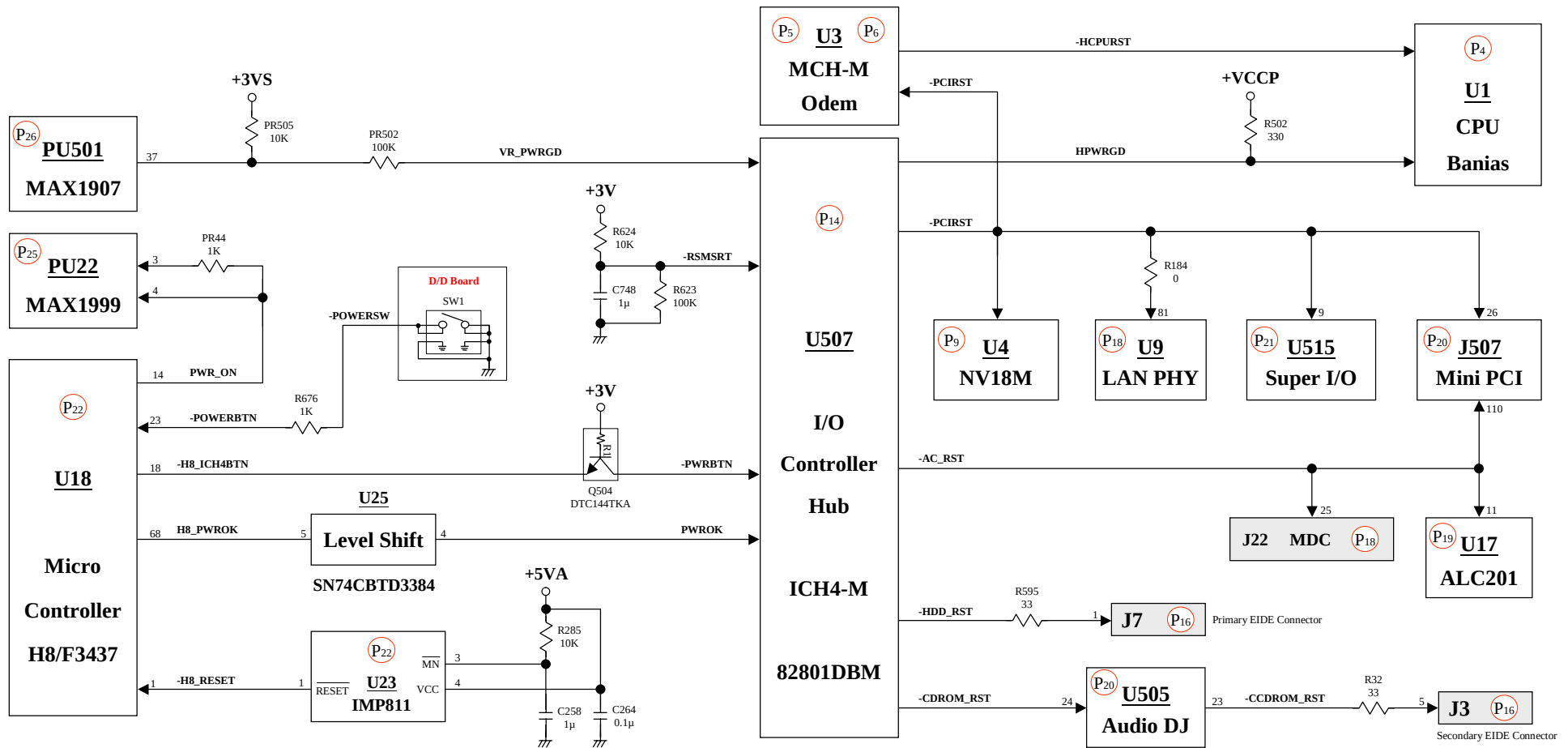
***** System Clock Check *****



8060B N/B Maintenance

8.2 No Display

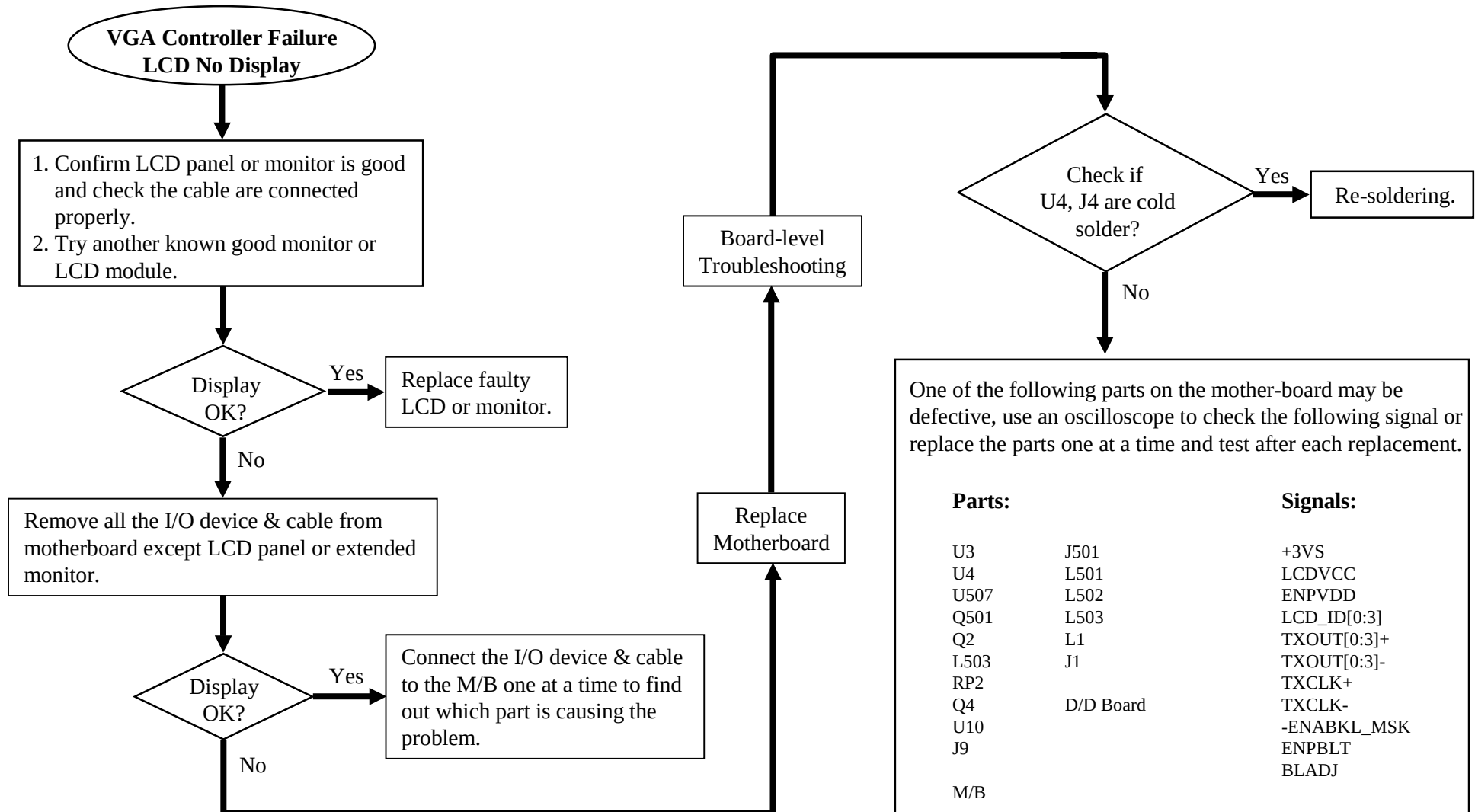
***** Power Good & Reset Circuit Check *****



8060B N/B Maintenance

8.3 VGA Controller Failure LCD No Display

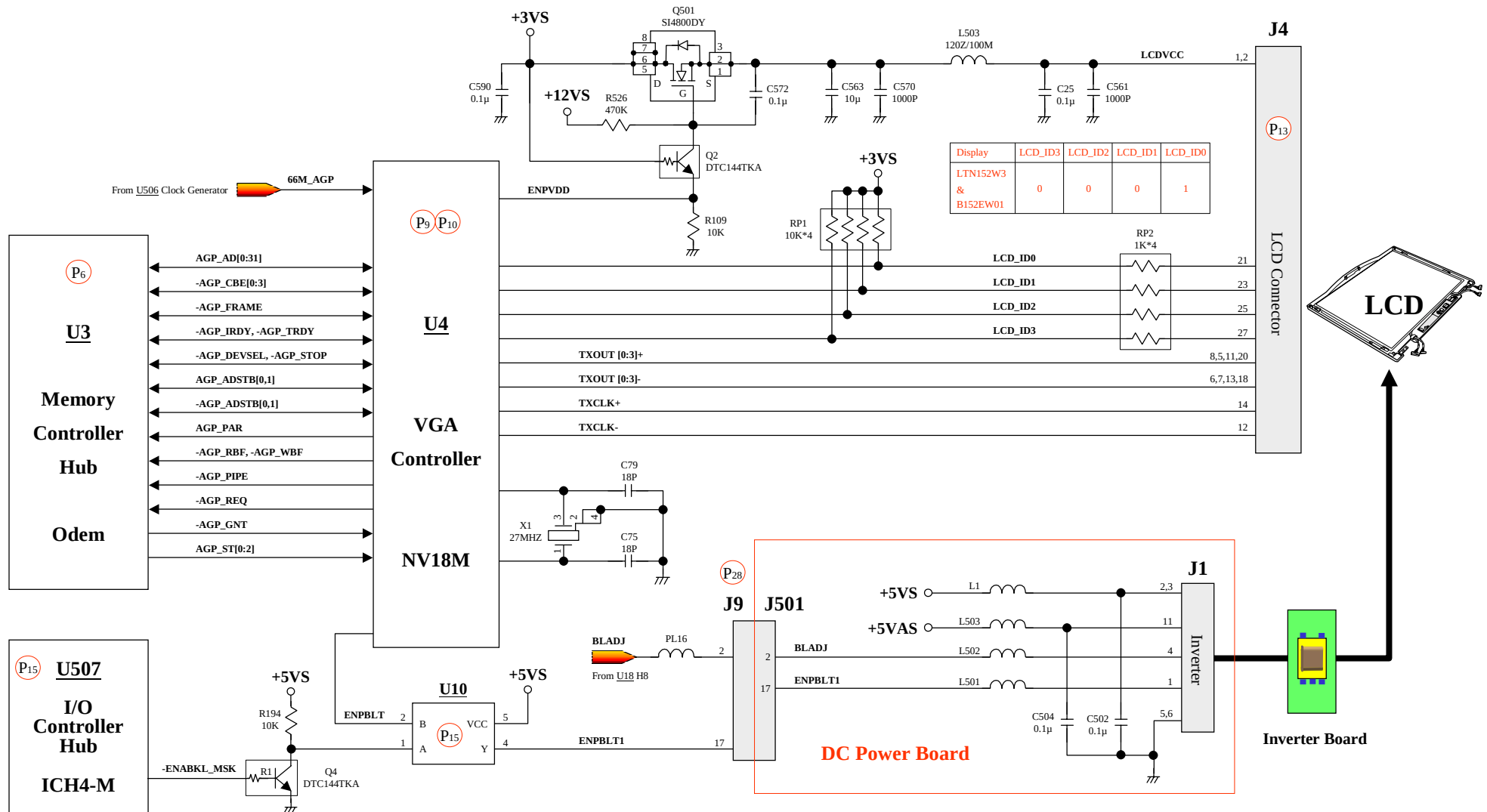
There is no display or picture abnormal on LCD although power-on-self-test is passed.



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8.3 VGA Controller Failure LCD No Display

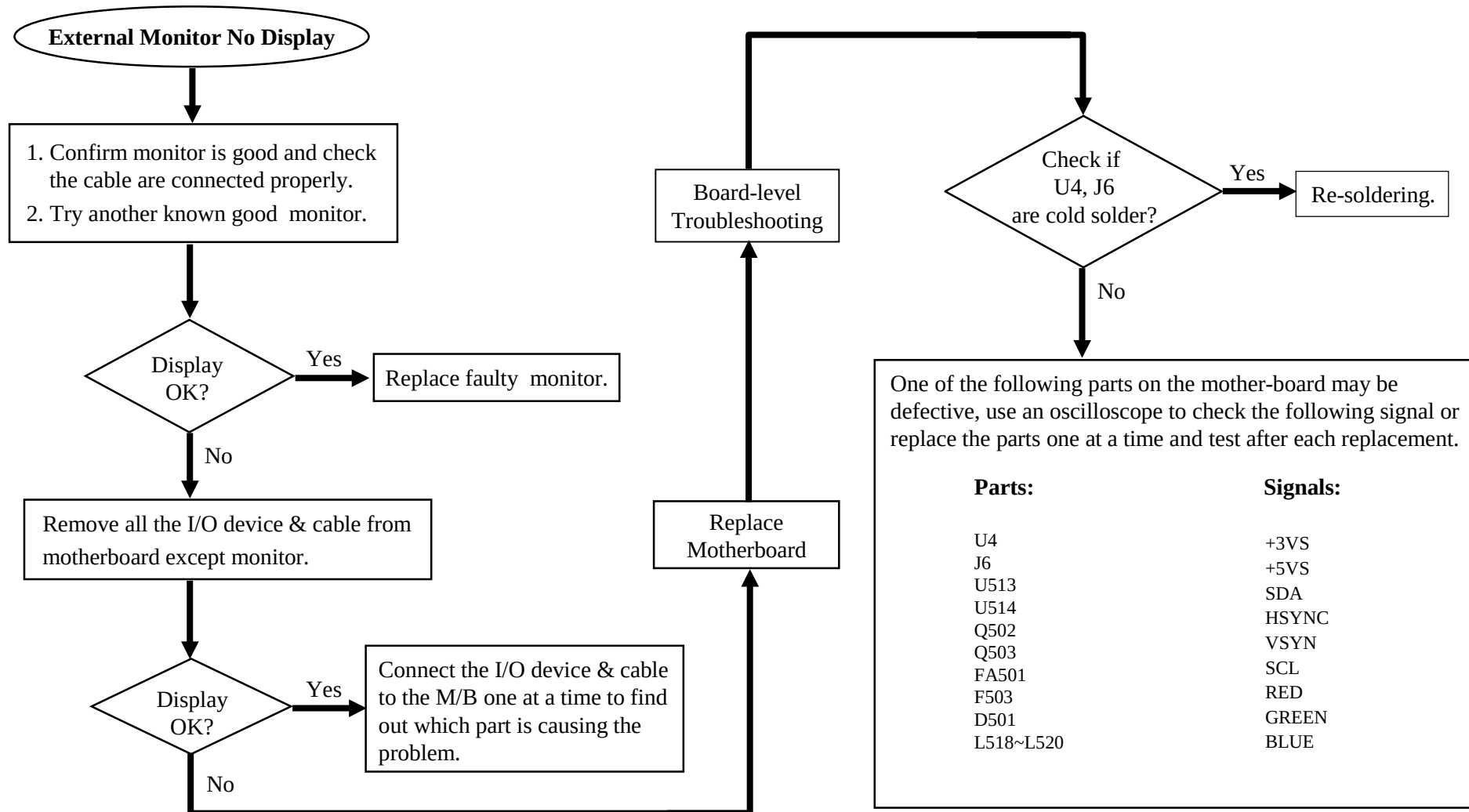
There is no display or picture abnormal on LCD although power-on-self-test is passed.



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8.4 External Monitor No Display

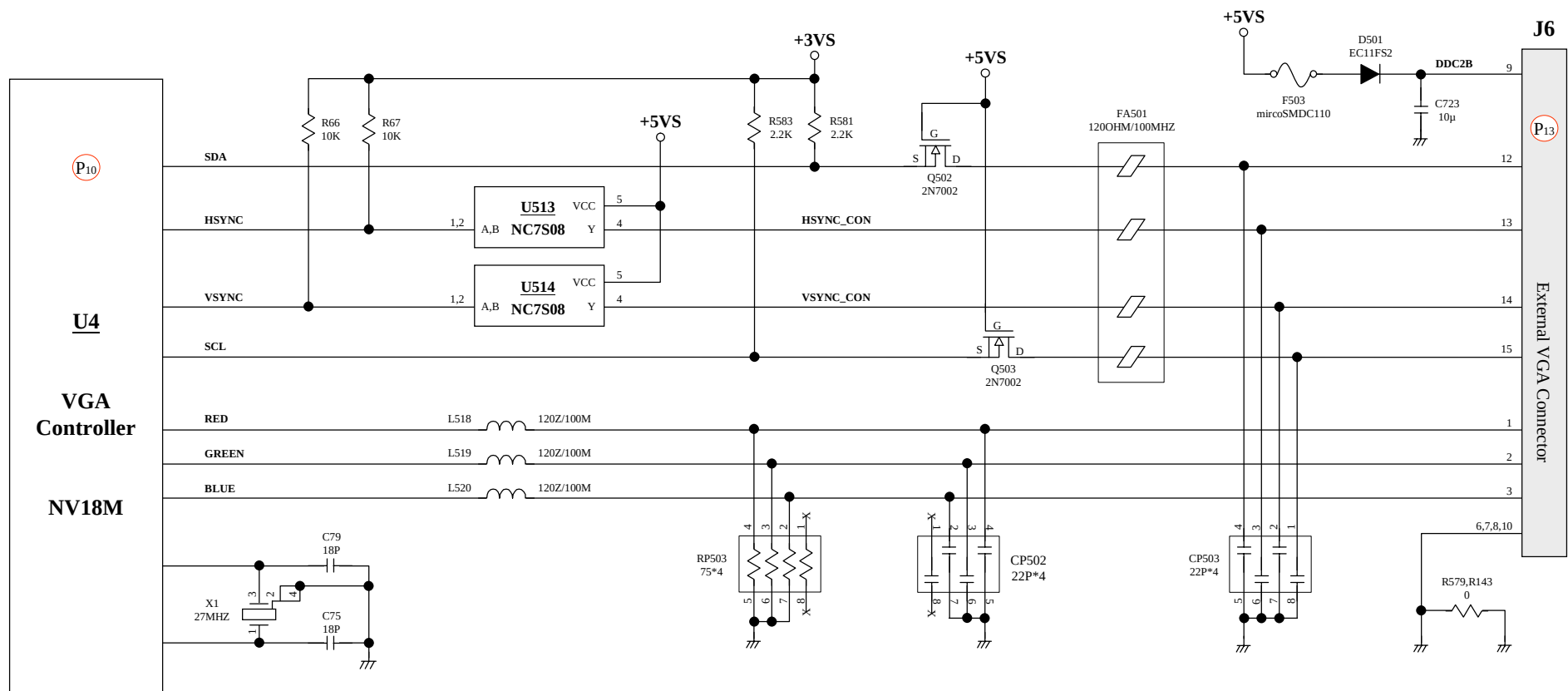
There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8060B N/B Maintenance

8.4 External Monitor No Display

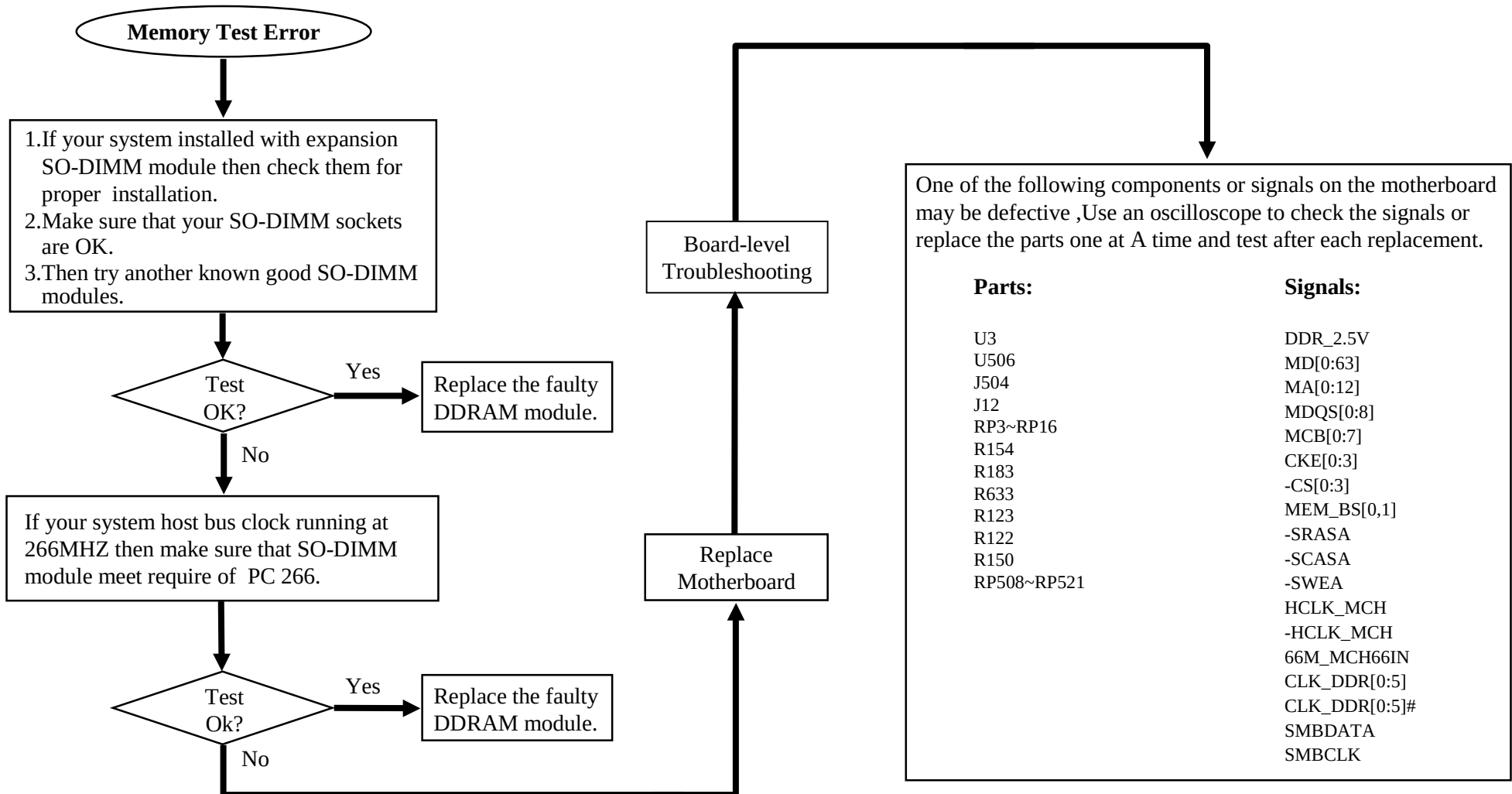
There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



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8.5 Memory Test Error

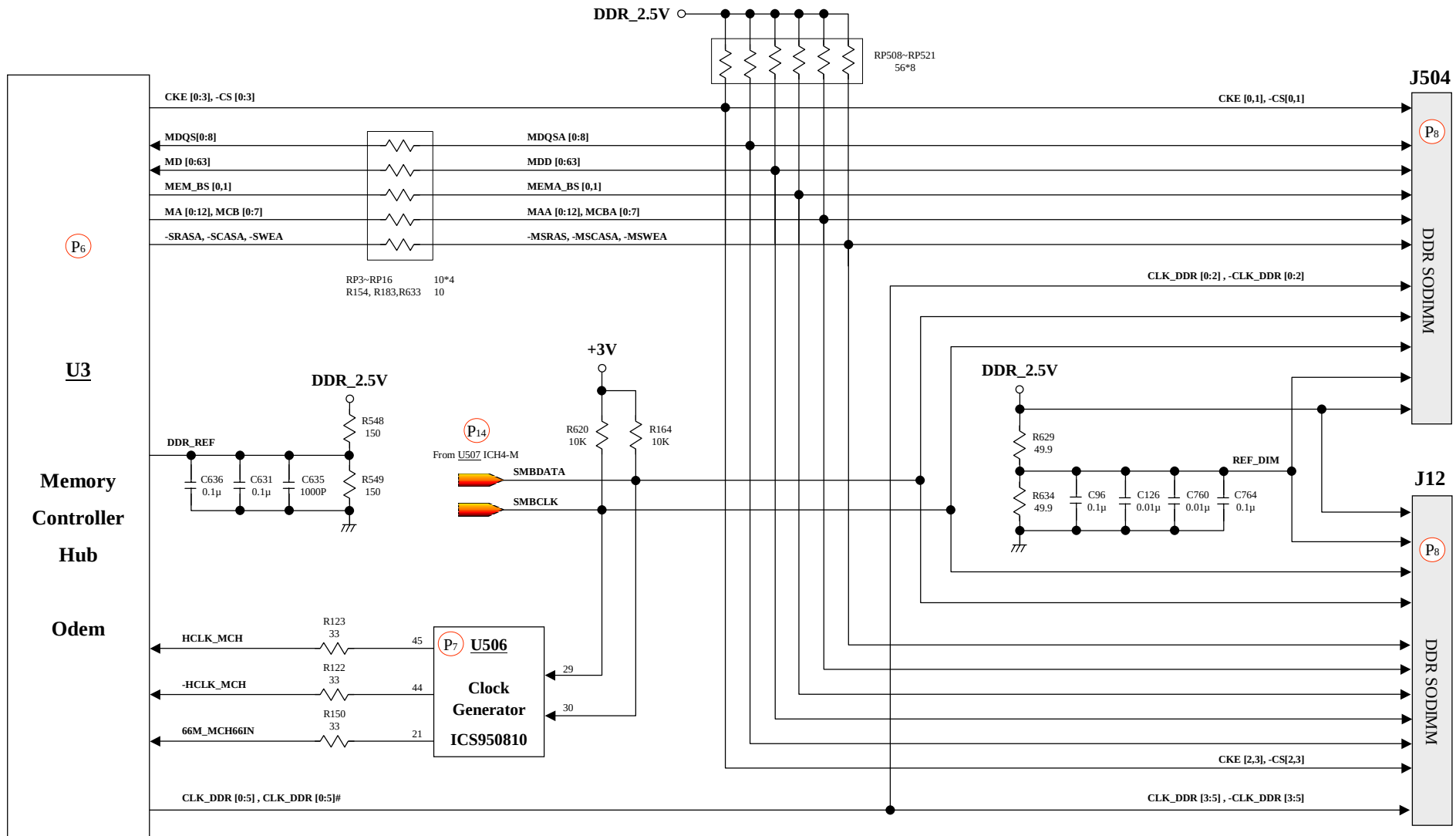
Extend DDRAM is failure or system hangs up.



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8.5 Memory Test Error

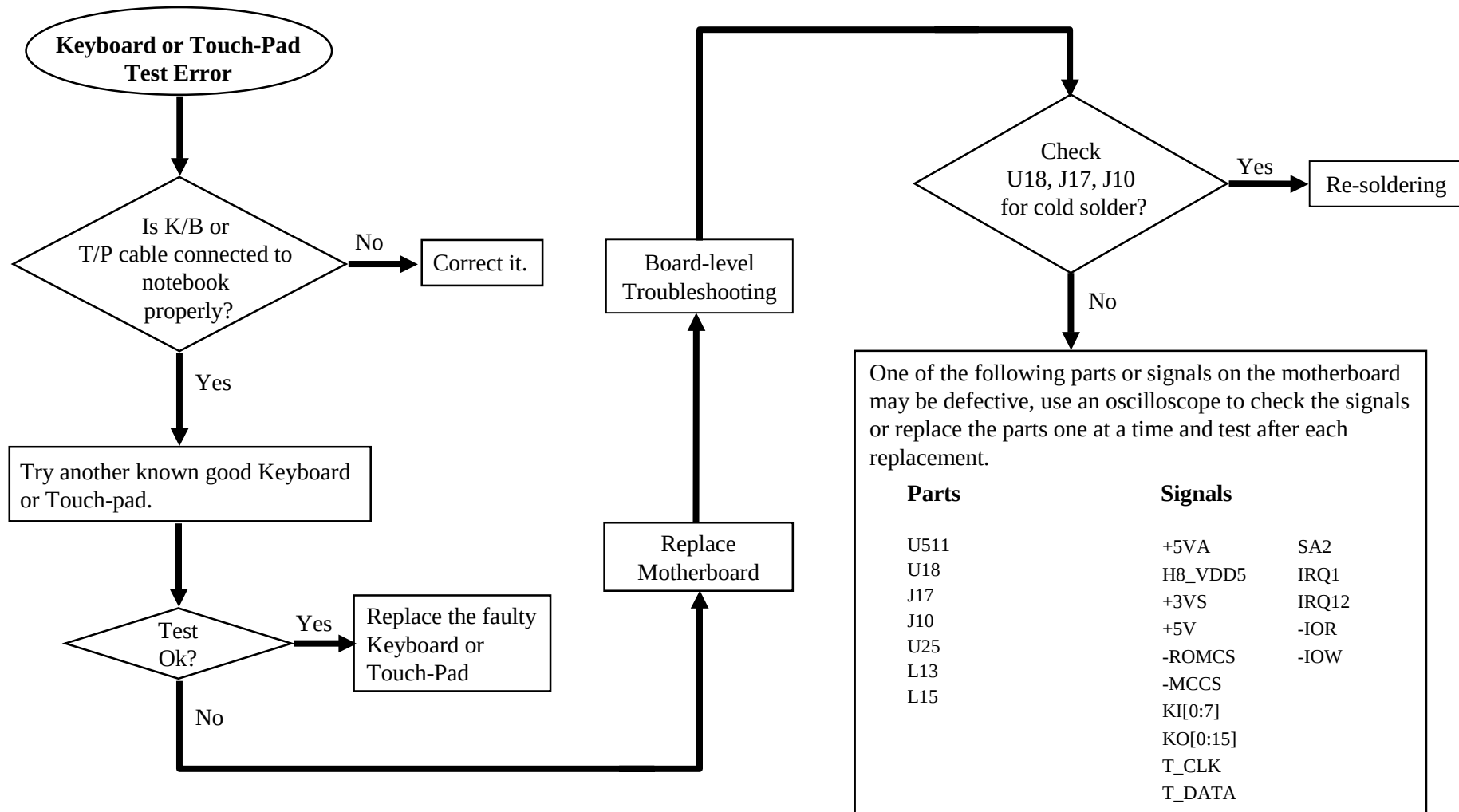
Extend DDRAM is failure or system hangs up.



8060B N/B Maintenance

8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

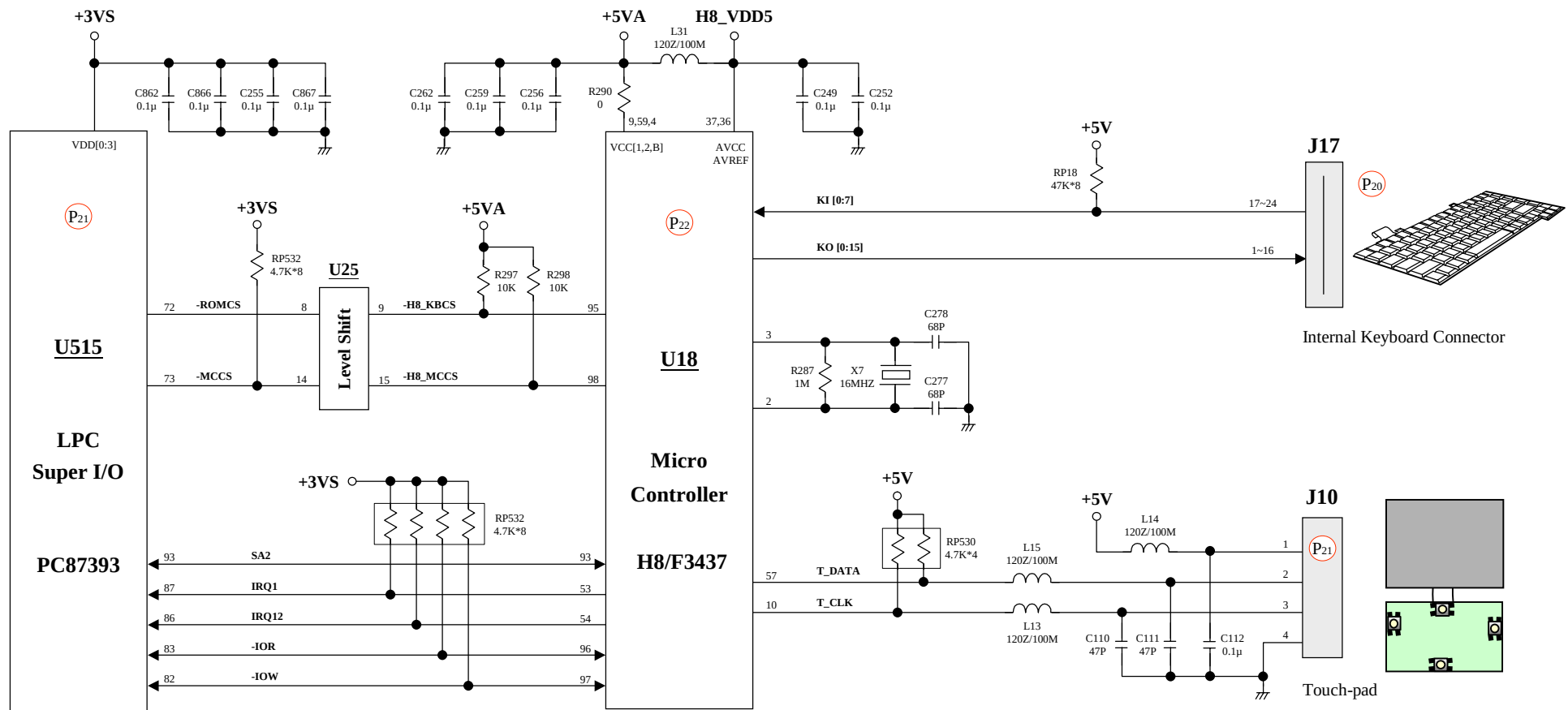
Error message of keyboard or touch-pad failure is shown or any key does not work.



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8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

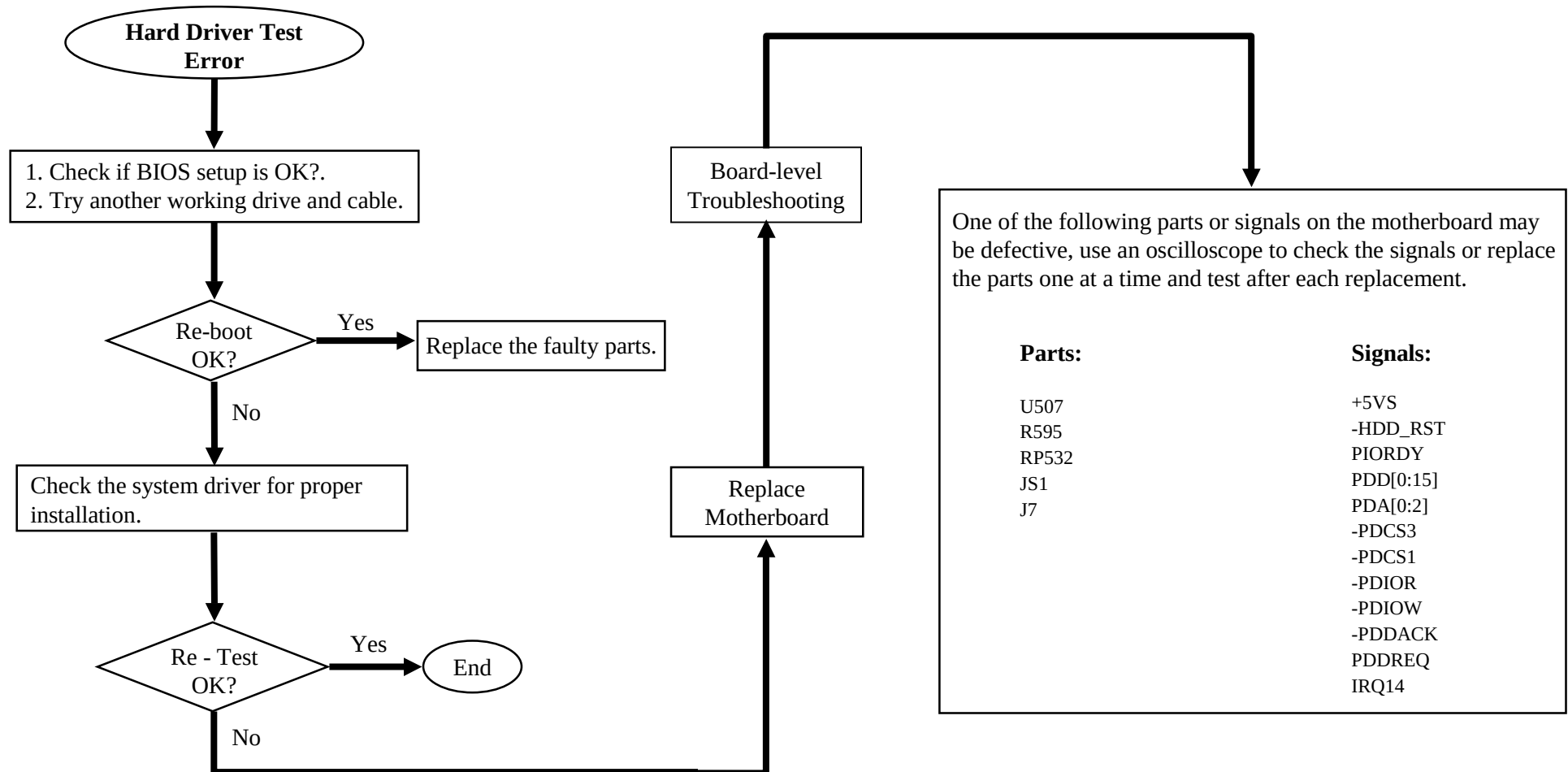
Error message of keyboard or touch-pad failure is shown or any key does not work.



8060B N/B Maintenance

8.7 Hard Drive Test Error

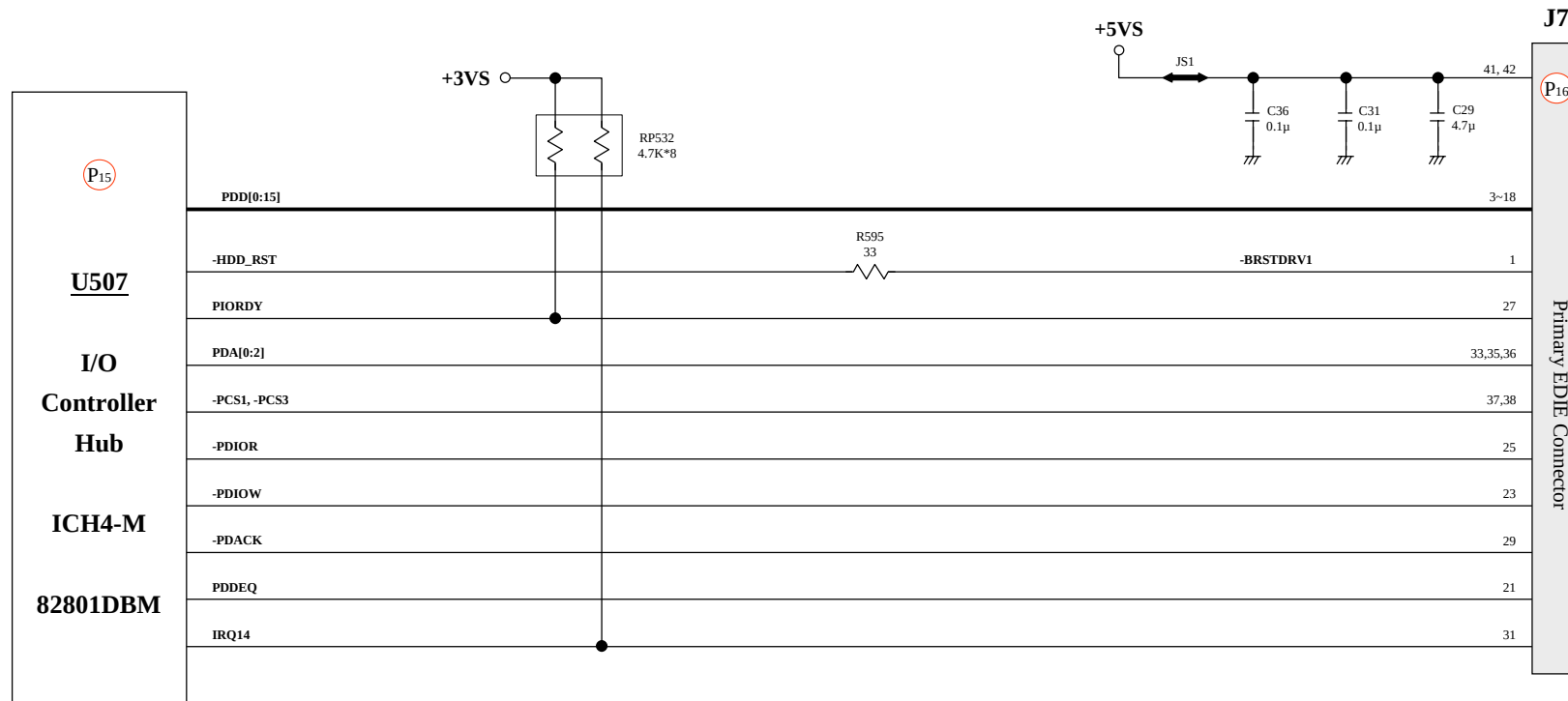
Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



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8.7 Hard Drive Test Error

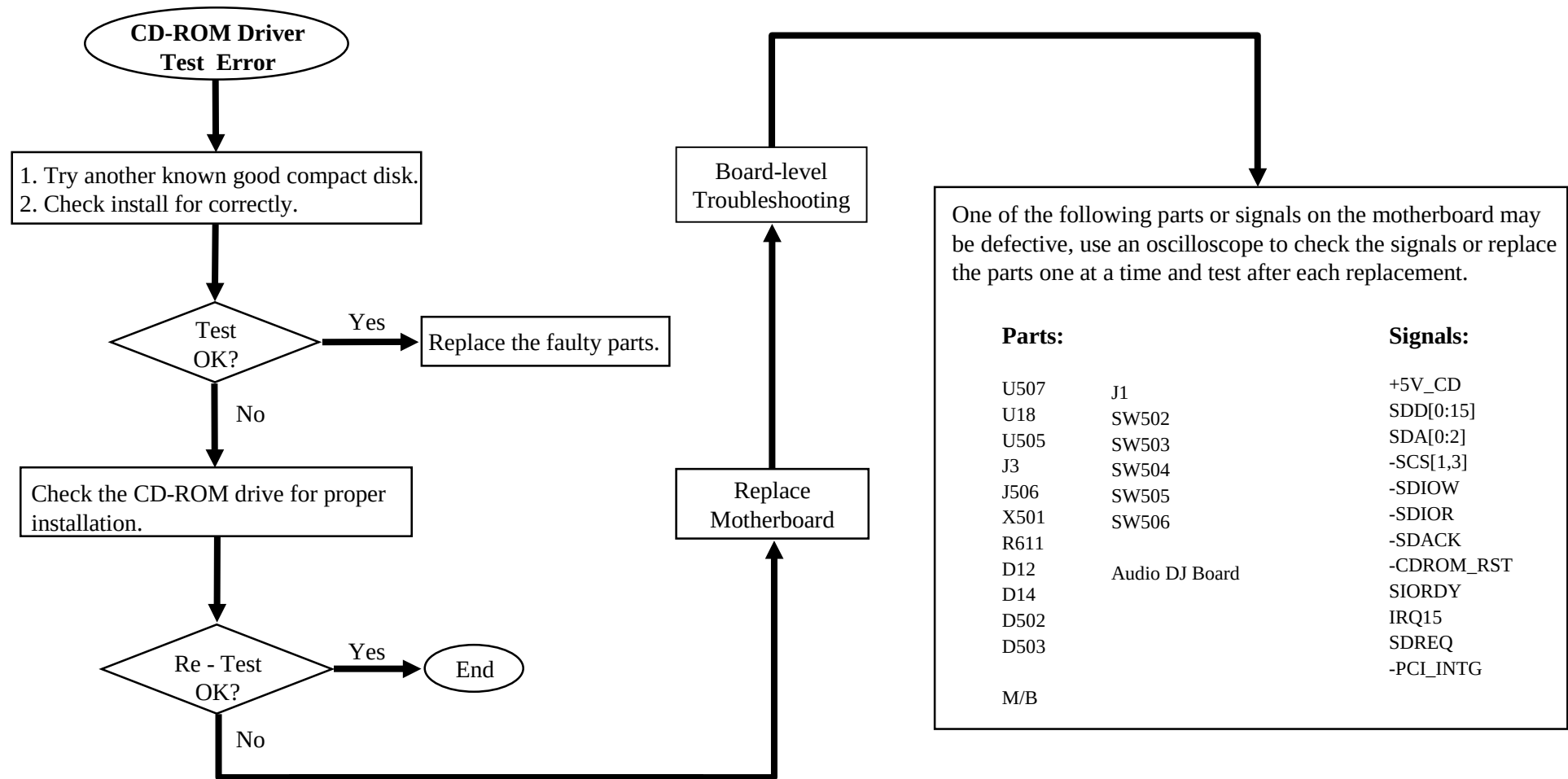
Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



8060B N/B Maintenance

8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.

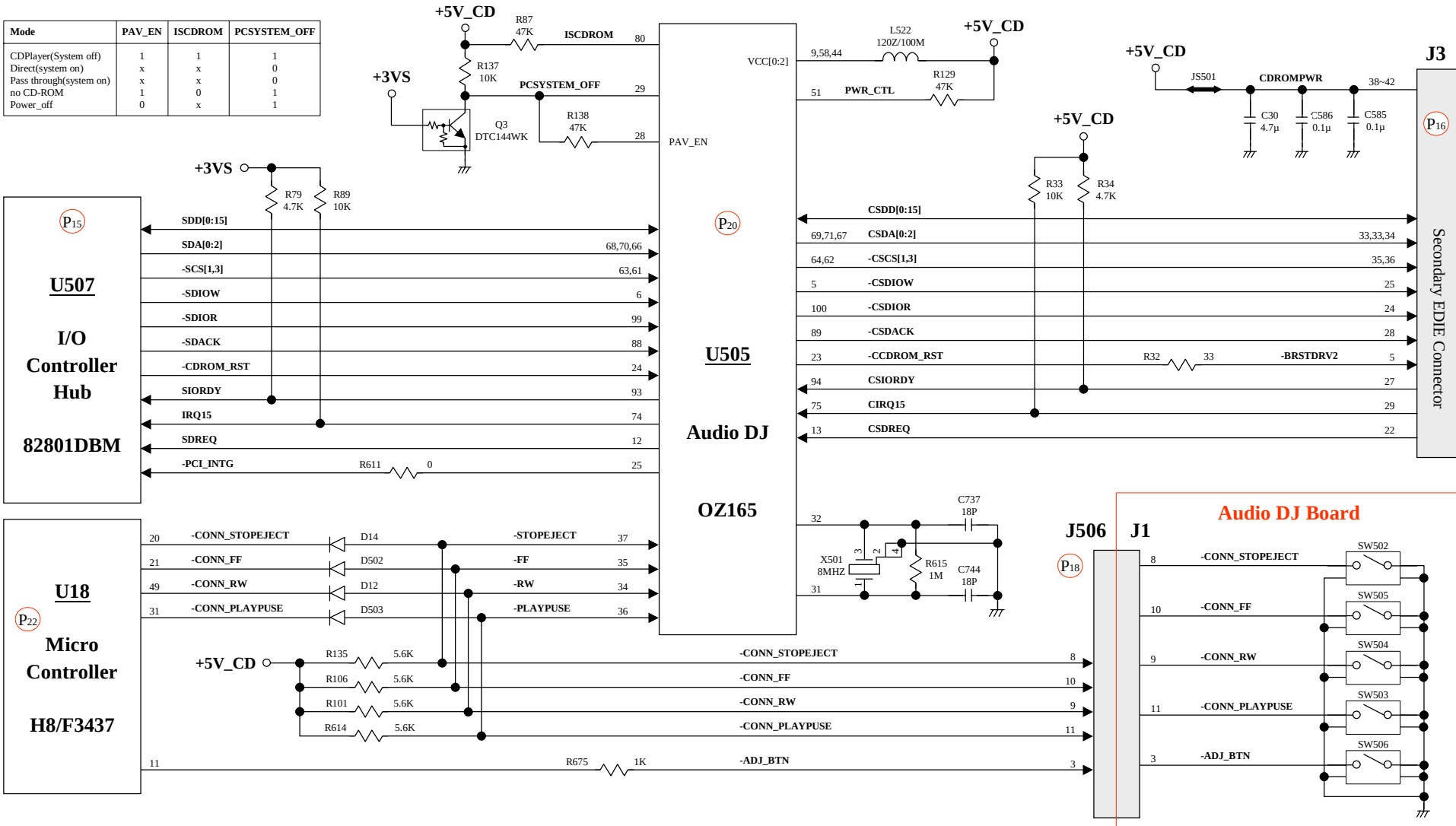


8060B N/B Maintenance

8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.

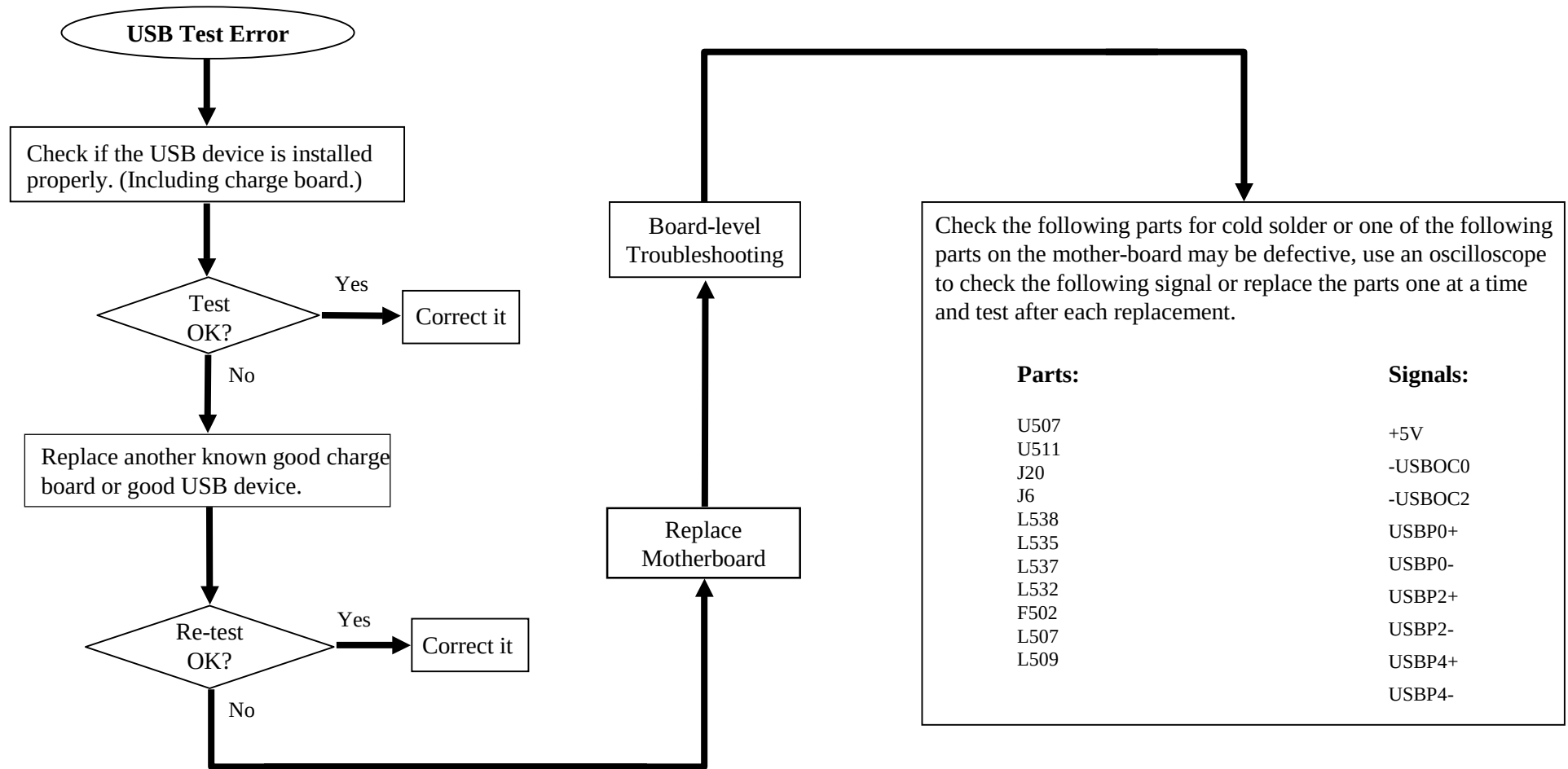
Mode	PAV_EN	ISCDROM	PCSYSTEM_OFF
CDPlayer(System off)	1	1	1
Direct(system on)	x	x	0
Pass through(system on)	x	x	0
no CD-ROM	1	0	1
Power_off	0	x	1



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8.9 USB Test Error

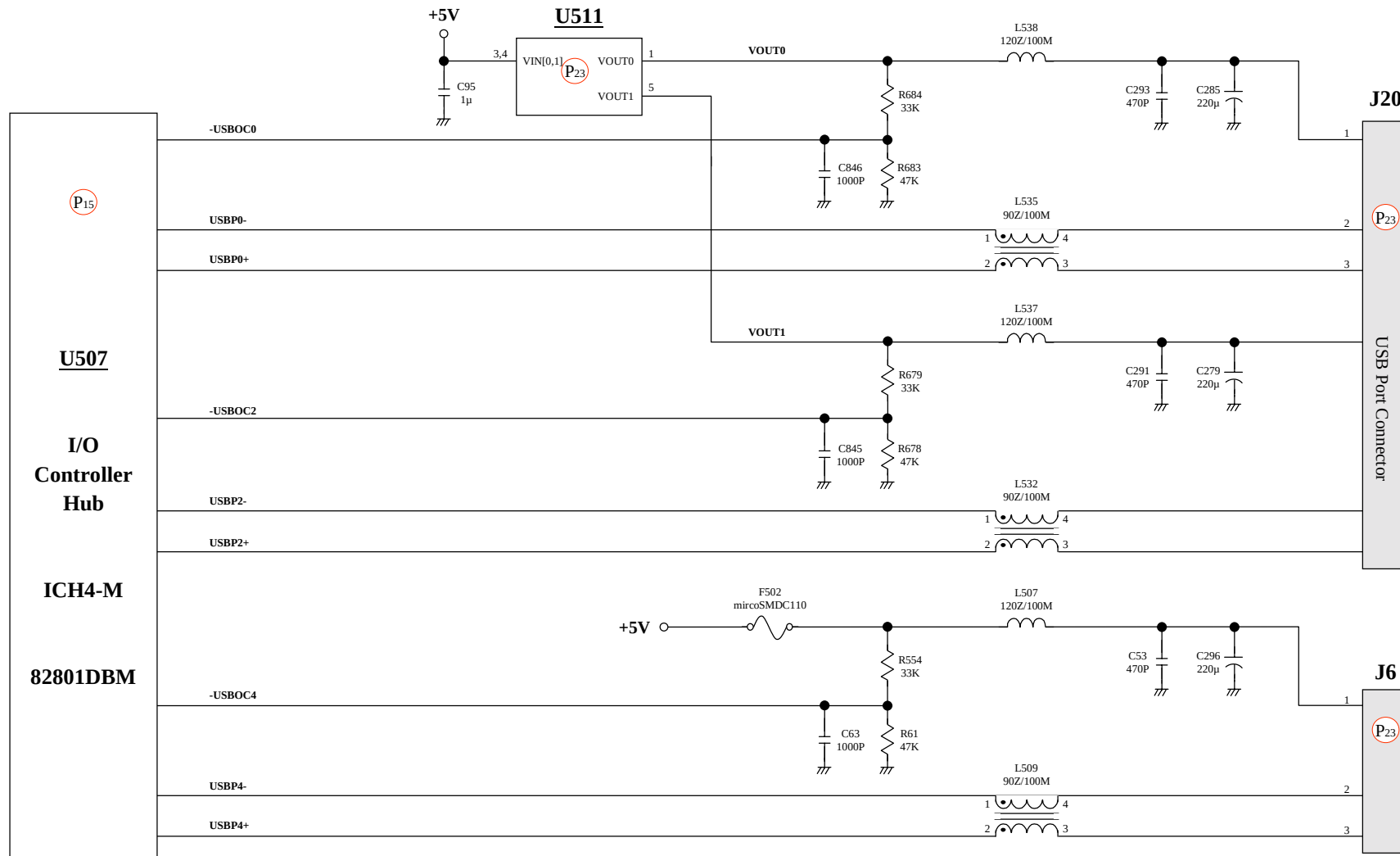
An error occurs when a USB I/O device is installed.



8060B N/B Maintenance

8.9 USB Test Error

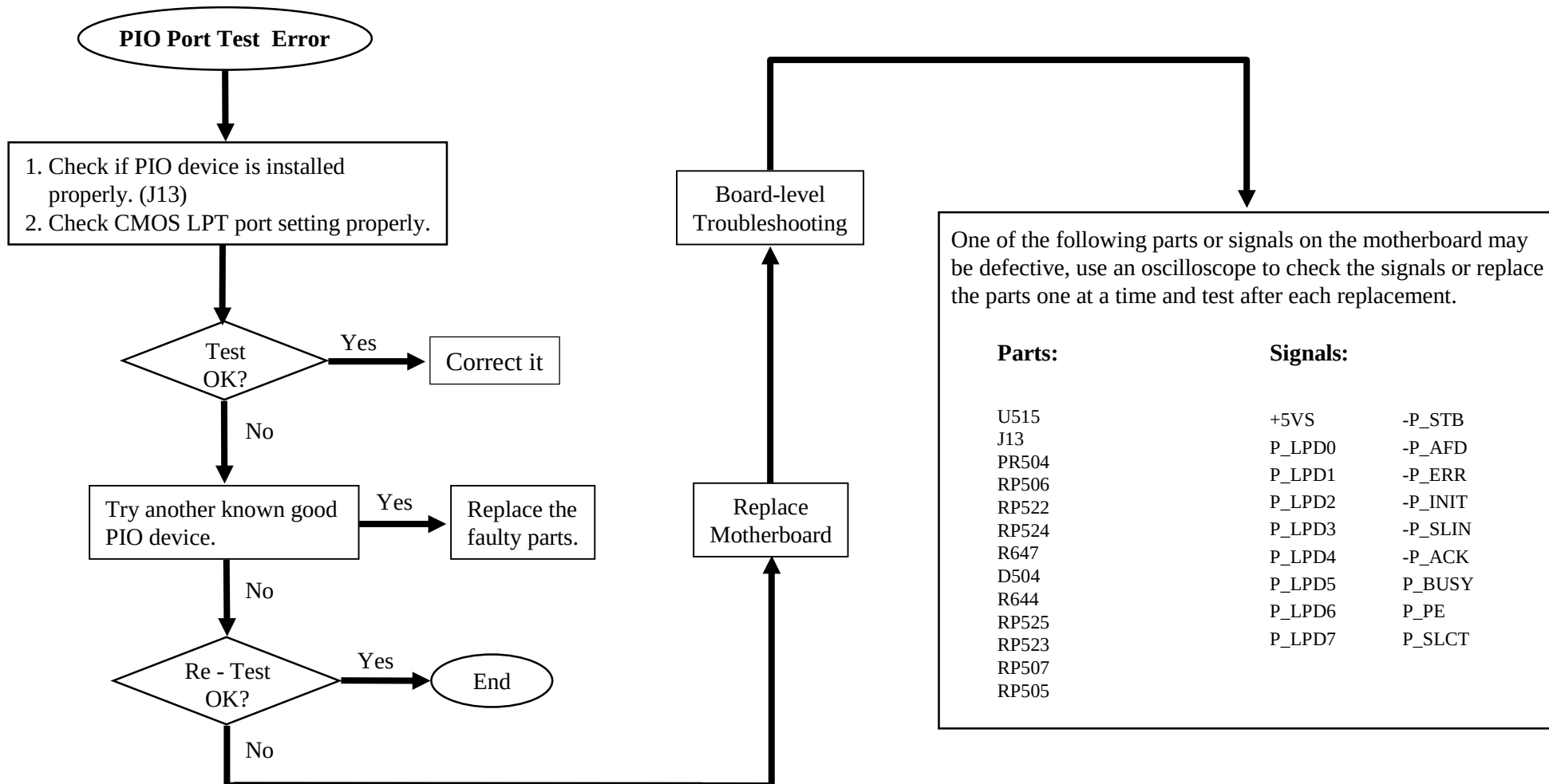
An error occurs when a USB I/O device is installed.



8060B N/B Maintenance

8.10 PIO Port Test Error

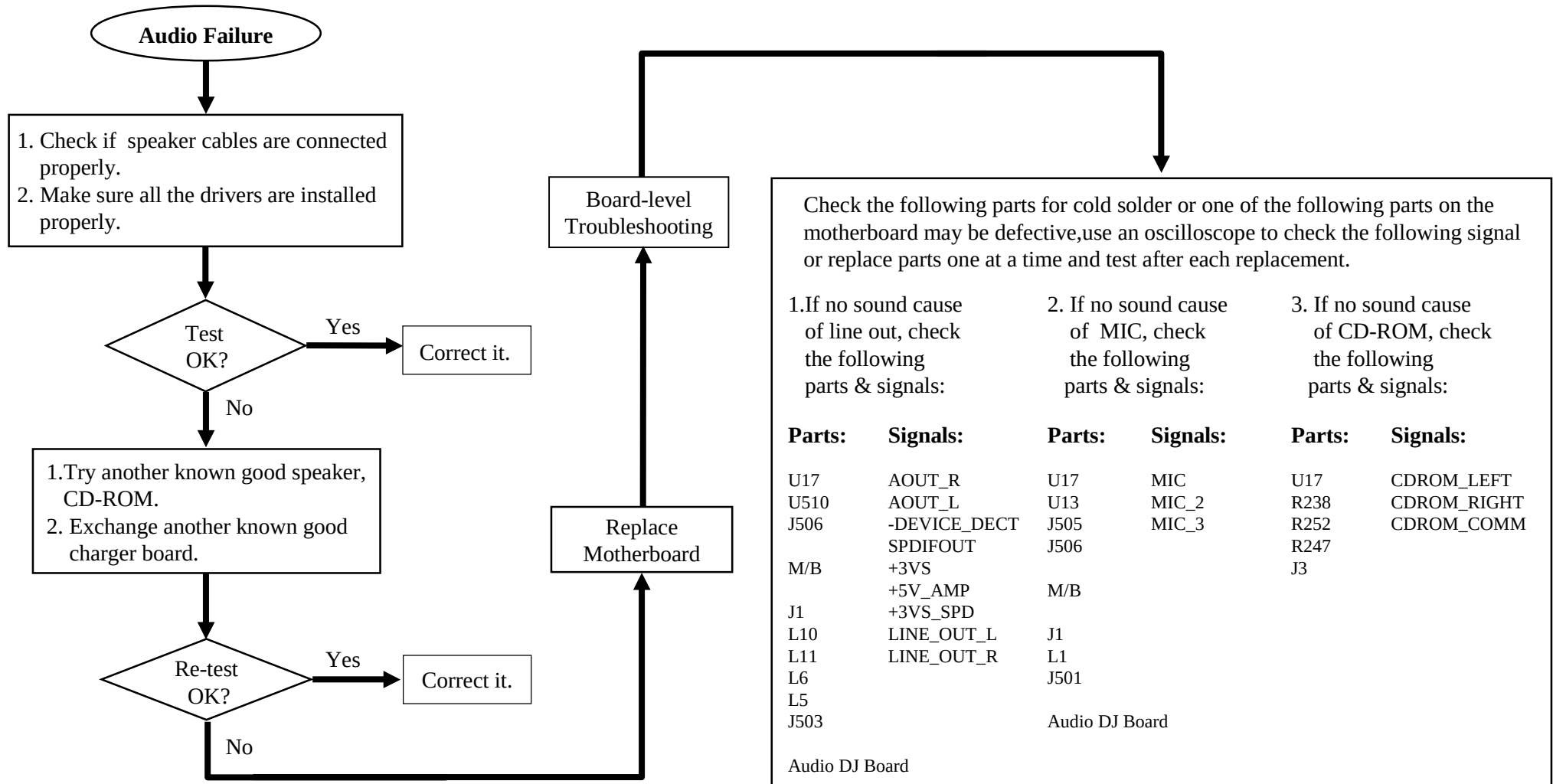
When a print command is issued, printer prints nothing or garbage.



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8.11 Audio Failure

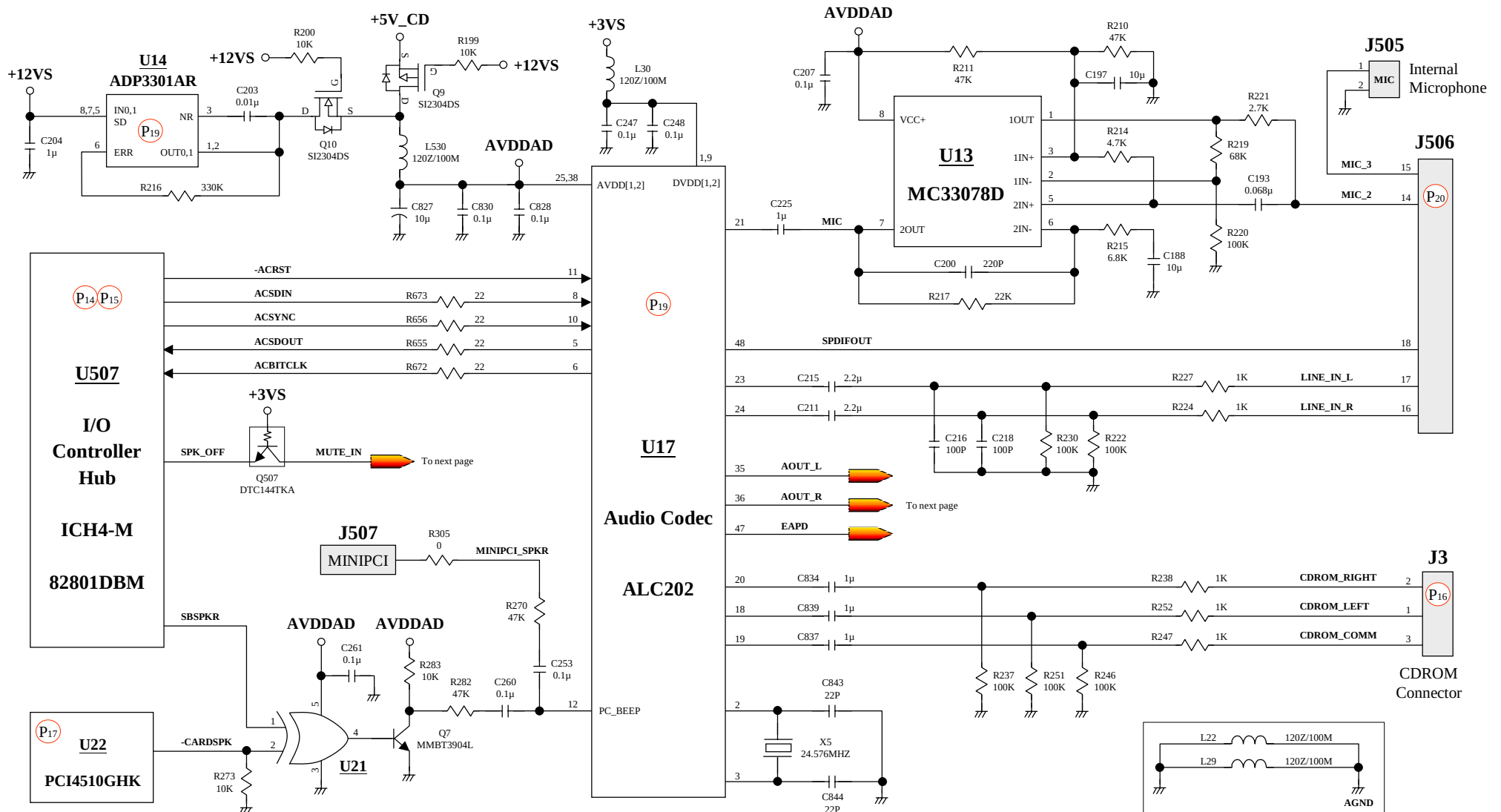
No sound from speaker after audio driver is installed.



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8.11 Audio Failure – Audio IN

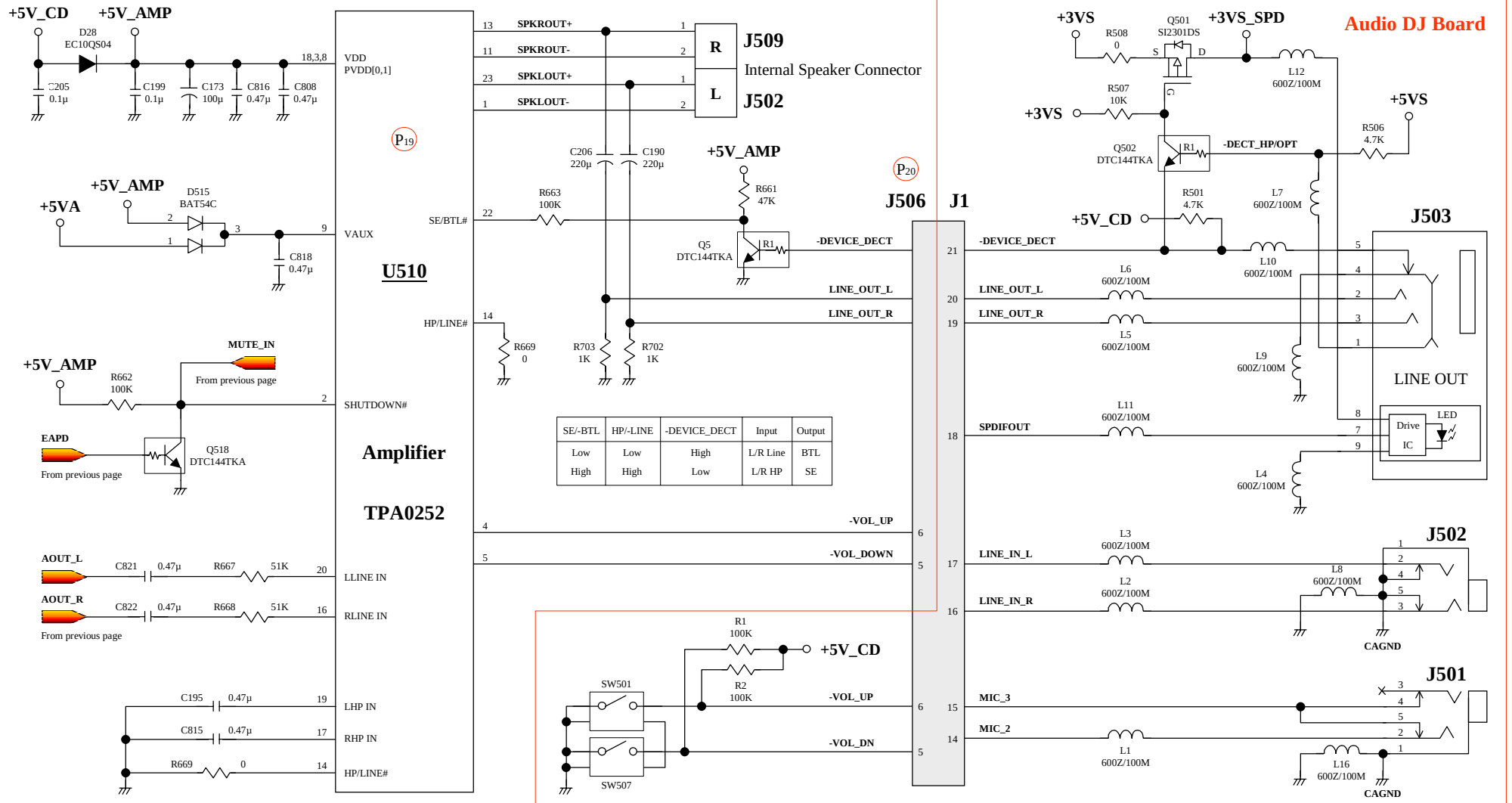
No sound from speaker after audio driver is installed.



8060B N/B Maintenance

8.11 Audio Failure – Audio OUT

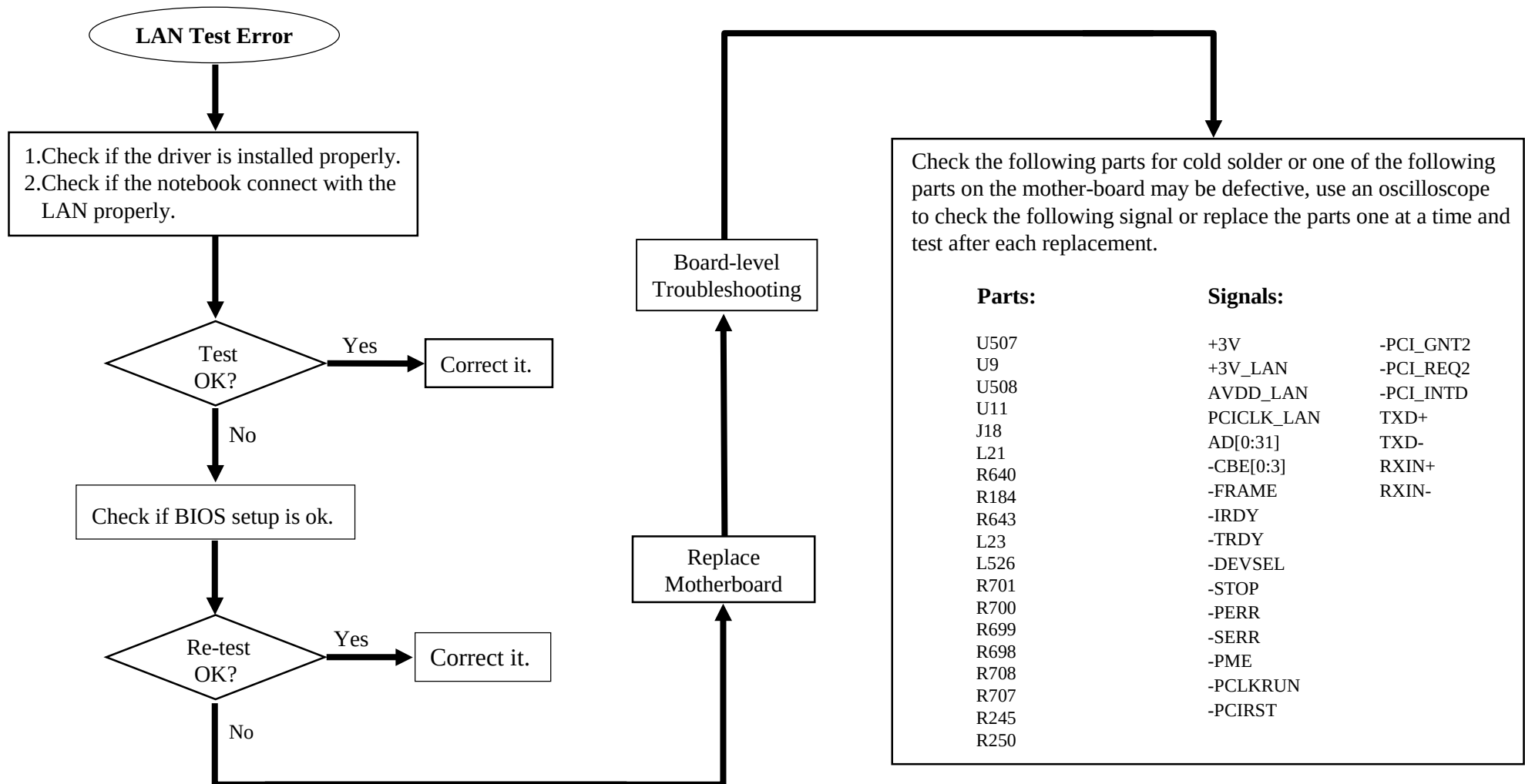
No sound from speaker after audio driver is installed.



8060B N/B Maintenance

8.12 LAN Test Error

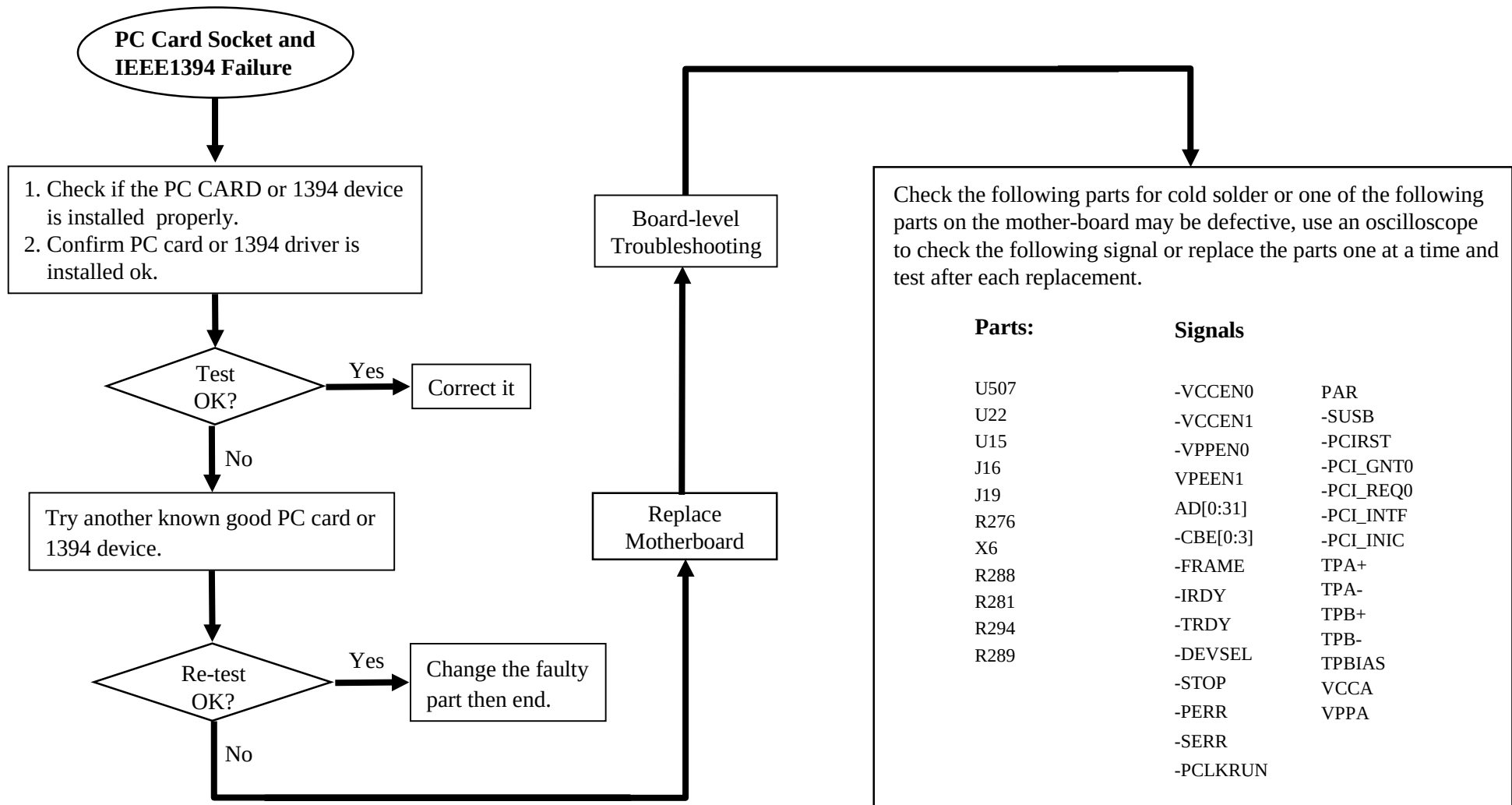
An error occurs when a LAN device is installed.



8060B N/B Maintenance

8.13 PC Card Socket and IEEE1394 Failure

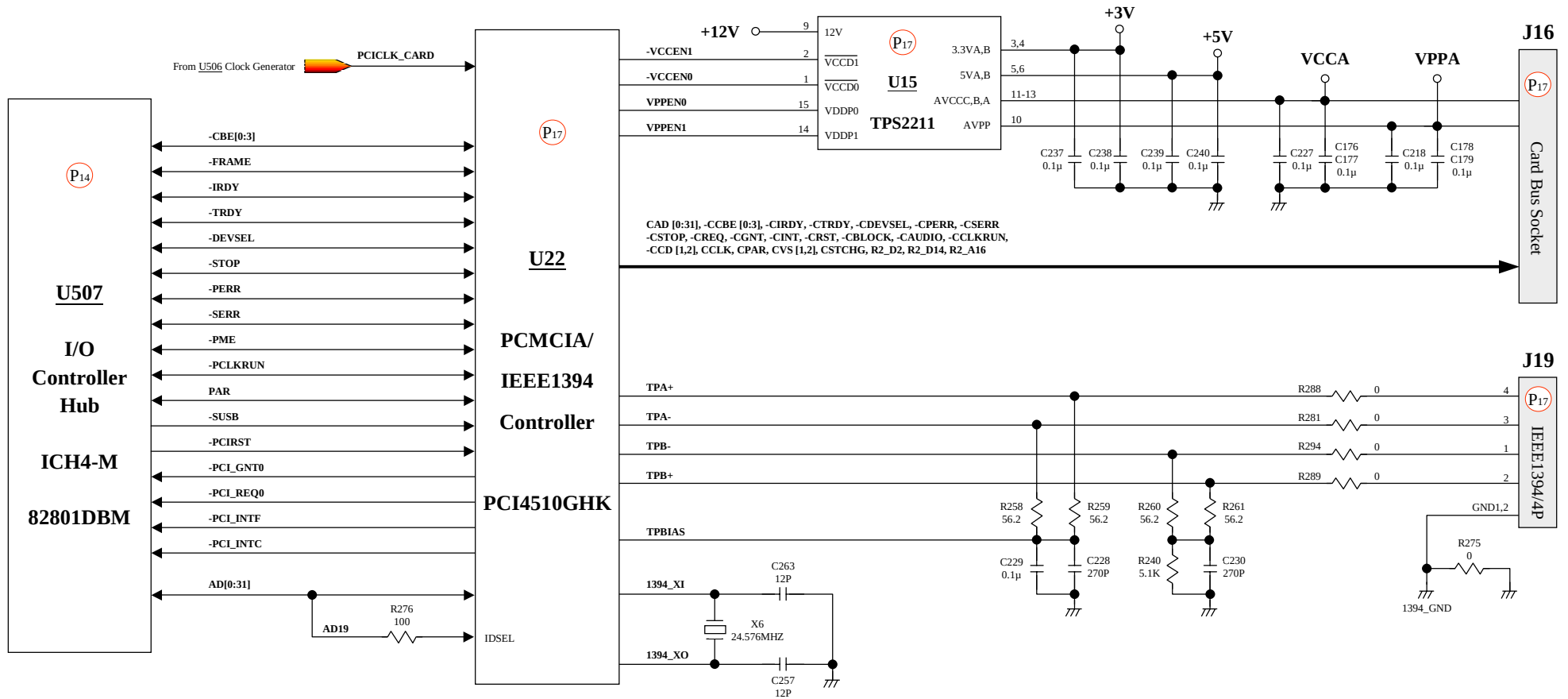
An error occurs when a PC card device or 1394 device is installed.



8060B N/B Maintenance

8.13 PC Card Socket and IEEE1394 Failure

An error occurs when a PC card device or 1394 device is installed.



8060B N/B Maintenance

9. Spare Parts List - 1

Part Number	Description	Location(S)
441999900211	AC ADPT ASSY OPTION;8060B	
442672600031	AC ADPT ASSY;19V,3.16A,DELTA,706	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
541667630032	AK;EN,8060B,UTILITY ONLY	
541667630031	AK;EN,BOX,8060B,UTILITY ONLY	
345673100034	AL-FOIL;LCD,8060	
422673100032	ANTENNA;LCD R,8060	
441999900073	BATT ASSY OPTION;LI,9-CELL,8060	
441504100001	BATT ASSY;LI,9CELLS/6AH,8060	
442673100003	BATT,ASSY;11.1V/6AH,LI-PANASONIC	
338536010006	BATTERY;LI,3.6V/2.0AH,18650,PANA	
340673100013	BEZEL ASSY;DVDROM,QSI,8060	
291000013019	BFM-SC,CON;HDR,FM,15P*2,1MM,ST,7	J8
291000810812	BFM-SC,CON;PHONE JACK,8P,R/A,RJ4	J18
291000410204	BFM-SC,CON;WFR,MA,2P,1.25,ST,SMT	J501,J502,J503,J505,J509
242670800113	BFM-WORLD MARK;WINXP,7521N	
221673140001	BOX;AK,8060	
340673100004	BRACKET ASSY;TP,8060	
342670500012	BRACKET;CD-ROM,TETRA	
342673100006	BRACKET;LCD LEFT,8060	
342673100007	BRACKET;LCD RIGHT,8060	
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z C	
421673400005	CABLE ASSY;TV-OUT,8640S	
272072153401	CAP;:015U ,CR,16V,10%,0603,X7R,S	C618

Part Number	Description	Location(S)
272075103403	CAP;:01U ,50V,10%,0603,X7R,SMT	C3,C16
272075103403	CAP;:01U ,50V,10%,0603,X7R,SMT	C20,C21,C22
272075103702	CAP;:01U ,50V,+80-20%,0603,Y5V,S	C126,C143,C153,C155,C203,C760
272075103401	CAP;:01U ,CR,50V ,10%,0603,X7R,S	C23,C45,C46,C503,C504,C557,C5
272075103401	CAP;:01U ,CR,50V ,10%,0603,X7R,S	PC17,PC3,PC503,PC505,PC513,P
272073223401	CAP;:022U,CR,25V ,10%,0603,X7R,S	C27,C32,C49,C52,C577,C579,C62
272072473402	CAP;:047U,16V ,10%,0603,X7R,SMT	C128,C634,C638,C640,C644,C811
272072473401	CAP;:047U,16V ,10%,0603,X7R,SMT	C7
272003683401	CAP;:068U,CR,25V ,10%,0805,X7R	C193
272073104703	CAP;:1U ,25V,+80-20%,0603,X7R,S	C1,C4
272075104701	CAP;:1U ,50V,+80-20%,0603,Y5V,S	C100,C101,C102,C103,C104,C112
272075104701	CAP;:1U ,50V,+80-20%,0603,Y5V,S	C501,C502,C503,C504,PC12,PC13
272075104703	CAP;:1U ,50V,+80-20%,0603,Y5V,S	C24,C26,C4,C6
272075104703	CAP;:1U ,50V,+80-20%,0603,Y5V,S	C3,C5
272072104402	CAP;:1U ,CR,16V,10%,0603,X7R,SM	C37,C39,C40,C43,C44,C50,C508,C
272072104402	CAP;:1U ,CR,16V,10%,0603,X7R,SM	PC1
272072224701	CAP;:22U ,16V ,+80-20%,0603,Y5V,	C633
272072334701	CAP;:33U ,CR,16V ,+80-20%,0603,Y	C9
272072474501	CAP;:47U ,16V ,20%,0603,Y5V,SMT	C195,C808,C809,C814,C815,C816
272072474501	CAP;:47U ,16V ,20%,0603,Y5V,SMT	PC518,PC524
272072474701	CAP;:47U ,16V,+80-20%,0603,Y5V,S	C23,C28
272072474701	CAP;:47U ,16V,+80-20%,0603,Y5V,S	C1
272002474401	CAP;:47U ,CR,16V ,10%,0805,X7R,S	C13,C14
272075102701	CAP;:1000P,50V ,+/-20%,0603,X7R,S	C222,C561,C570,C63,C825,C826,C
272075102701	CAP;:1000P,50V ,+/-20%,0603,X7R,S	PC11,PC16,PC507

8060B N/B Maintenance

9. Spare Parts List - 2

Part Number	Description	Location(S)
627207510241	CAP;1000P,50V,10%,0603,X7R,SMT	C25
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TU	C11,C196,C5
272075102402	CAP;1000P,CR,50V,10%,0603,X7R,IN	C635,PC19
272075101701	CAP;100P,50V,+/-10%,0603,NPO,S	C213,C216
272075101401	CAP;100P,50V,10%,0603,COG,SMT	C33,C34,C35,C735,C87,C88,C94,C
272075101401	CAP;100P,50V,10%,0603,COG,SMT	PC18,PC520
272075101401	CAP;100P,50V,10%,0603,COG,SMT	C501,C502,C503
272431105901	CAP;100U,10V,20%,7343,SMT	C173
272075100701	CAP;10P,50V,+/-10%,0603,NPO,SM	C105,C107,C108,C109,C116,C167
272021106501	CAP;10U,10V,20%,1210,X7R,SMT	PC2,PC39,PC4,PC48,PC53,PC538
272021106501	CAP;10U,10V,20%,1210,X7R,SMT	PC516,PC517
272011106701	CAP;10U,10V,+80-20%,1206,Y5V,S	PC504,PC511,PC521,PC522,PC52
272011106407	CAP;10U,10V,+/-10%,1206,X5R,SMT,	C151,C165,C188,C197,C212,C563
272043106401	CAP;10U,25V,+/-10%,1812,X5R,SMT,T	PC49,PC59
272993106001	CAP;10U,25V,2.2mm,X5R,KYOCERA,SM	PC25,PC28,PC539,PC545,PC560,
272011106404	CAP;10U,6.3V,10%,1206,X7R,SMT	C1,C10,C12,C122,C13,C14,C144,C
272075120301	CAP;12P,CR,50V,5%,0603,NPO,S	C118,C119,C257,C263
272431156501	CAP;150U,6.3V,TPE,20%,7343,SMT	C871,PC37,PC41,PC65,PC67
272433156502	CAP;15U,TQC,25V,20%,H=1.9,7343	PC504,PC505,PC506,PC531,PC55
272433156502	CAP;15U,TQC,25V,20%,H=1.9,7343	PC13,PC14
272075181301	CAP;180P,50V,5%,0603,NPO,SMT	C166
272073180401	CAP;18P,CR,25V,10%,0603,NPO,S	C277,C278,C737,C744,C75,C79
272071105701	CAP;1U,CR,10V,80-20%,0603,Y5	C141,C161,C164,C170,C204,C224
272002105403	CAP;1U,CR,16V,10%,0805,X7R,SM	C6
272003105701	CAP;1U,CR,25V,+80%-20%,0805,	PC13,PC532,PC68,PC69,PC88,PC

Part Number	Description	Location(S)
272003105701	CAP;1U,CR,25V,+80%-20%,0805,	PC519
272071105403	CAP;1U,10V,10%,0603,X5R,SMT	C8
272001225401	CAP;2.2U,CR,10V,10%,0805,X7R,S	C5
272002225701	CAP;2.2U,CR,16V,+80-20%,0805,Y	C211,C215,C629,C728,C729,C734
272012225702	CAP;2.2U,CR,16V,+80-20%,1206,Y	C145,C187,C273,C289,C738
272075222701	CAP;2200P,50V,+/-20%,0603,X7R,S	C546,C645,C663,C667,C676,C677
272075221401	CAP;220P,CR,50V,10%,0603,X7R,S	C200,C28,C54,C55,C559,C593,C5
272431227402	CAP;220U,2V,-35/+10%,H1.9,S,SP-C	PC20,PC36,PC501,PC524,PC565,
272431227402	CAP;220U,2V,-35/+10%,H1.9,S,SP-C	PC501,PC509
272421225501	CAP;220U,TPE,4V,20%,7343,SMT	PC27,PC55,PC56
272421225501	CAP;220U,TPE,4V,20%,7343,SMT	PC10,PC9
272075220701	CAP;22P,50V,+/-10%,0603,NPO,S	C843,C844
272075220701	CAP;22P,50V,+/-10%,0603,NPO,S	C11
272021226701	CAP;22U,10V,+80-20%,1210,Y5V,S	C138,C149,C156,C797
272041226501	CAP;22U,CR,10V,20%,1812,X7R,S	C672,C679
272011226701	CAP;22U,CR,10V,1206,Y5V,+80~20%	C872
272075271401	CAP;270P,50V,+/-10%,0603,X7R,SMT	C174,C194,C217,C228,C230,C241
272075209001	CAP;2P,CR,50V,+/-0.25PF,0603,	C13
272075330401	CAP;33P,CR,50V,10%,0603,X7R,S	C573,C583,C597
272001475701	CAP;4.7U,CR,10V,+80-20%,0805,Y	C114,C56,C620,C642,C659,C66,C
272012475701	CAP;4.7U,CR,16V,+80-20%,1206,Y	C147,C29,C30,C647
272012475502	CAP;4.7U,CR,16V,20%,1206,Y5U,SM	C14
272013475701	CAP;4.7U,CR,25V,+80-20%,1206,Y	C2
272075472701	CAP;4700P,50V,+/-20%,0603,X7R,S	C42,C48,C51,C587,C589,C59,C59
272075471401	CAP;470P,50V,10%,0603,X7R,SMT	C291,C293,C41,C53,C62,C630,C6

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9. Spare Parts List - 3

Part Number	Description	Location(S)
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	PC2
272072471301	CAP;470P ,CR,16V ,5% ,0603,NPO,P	C12
272075470701	CAP;47P ,50V ,+ -10%,0603,NPO,S	C110,C111
272431476502	CAP;47U ,6.3V,20%,SP-CAP,7343,S	C2
272030680402	CAP;68P ,3KV,5%,1808,NPO,SMT,PR	C15
272431826501	CAP;82U ,2.5V,20%,SP-CON,7343,S	PC19
221673150002	CARD BOARD;FRAME,PALLET,8060	
221673150003	CARD BOARD;TOP/BTM,PALLET,8060	
221600020128	CARTON;380MM*320MM*320MM,BC FLUT	
221503220001	CARTON;BATTERY,GRAMPUS	
221673120003	CARTON;N-B,8060	
431676300001	CASE KIT;8060B	
335152000044	CFM-BAT;FUSE THERMAL 98°C	
342665500008	CFM-SUYIN;S-STANDOFF,#4-40H4.8,N	
324180786564	CFM-TCL;IC,CPU,PENTIUM-M,1.3G,uF	
412676300001	CFM-TCL;INTEL Clexico 802.11b;PR	
242676300001	CFM-TCL;LABEL,AGENCY-GLOBAL,8060	
273000500095	CHOCK COIL;0.5UH.1.0mOHM,25%,30A	PL1
273000500096	CHOCK COIL;4.7UH.20mOHM,25%,4.5A	PL18,PL25,PL3,PL6
273000500096	CHOCK COIL;4.7UH.20mOHM,25%,4.5A	PL503
273000500015	CHOKE COIL;50UH(REF),D.4*2,5,5T,	L3
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L509,L532,L535
361200001018	CLEANER;YC-336,LIQUID,STENCIL/P	
361200001018	CLEANER;YC-336,LIQUID,STENCIL/P	
331000007021	CON;BAT,7P,2.5mm,SUYIN	J21

Part Number	Description	Location(S)
291000001001	CON;BATTERY,10P,FM,2MM,R/A,SMT	
331000008080	CON;BATTERY,8P,2.5MM,ALLTOP,C103	
331720025012	CON;D,FM,25P,2.77,R/A,TITAN	J13
291000151204	CON;FPC/FFC,12P,.5MM,R/A,SMT,RED	J2
291000142406	CON;FPC/FFC,24P,0.5MM,H=2,R/A,SM	J506
291000142406	CON;FPC/FFC,24P,0.5MM,H=2,R/A,SM	J1
291000142402	CON;FPC/FFC,24P,1MM,H5.5,ST,ACES	J17
291000150411	CON;FPC/FFC,4P,1MM,R/A,SMT,85202	J1
291000150411	CON;FPC/FFC,4P,1MM,R/A,SMT,85202	J10
291000012411	CON;HDR,12P*1,1.25,ACES,SMT	J1
291000013022	CON;HDR,FM,15*2,2.54mm,3A,SMT	J501
291000013021	CON;HDR,FM,15P*2,0.8MM,ST,H=5.2,	J22
331040044017	CON;HDR,FM,22P*2,2MM,H=5.4,R/A,D	J7
331040050016	CON;HDR,FM,25P*2,0.8MM,H=2,R/A,D	J3
291000021101	CON;HDR,MA,11P*1,1.25,R/A,DF13-1	J1
291000013023	CON;HDR,MA,15*2,2.54mm,3A,SMT	J9
291000013016	CON;HDR,MA,15P*2,1MM,H4.25,ST,SM	J4
291000020202	CON;HDR,MA,2P*1,1.25,R/A,SMT,HIR	J14
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	J2
291000020304	CON;HDR,MA,3P,1.25MM,H3.5MM,R/A,	J1
331130004014	CON;HDR,SHR,MA,4P*1,H=7.3,R/A,US	J6
291000256821	CON;IC CARD,68P,635MM,62598-22A	J16
331000004009	CON;IEEE1394,MA,4P*1,0.8MM,R/A	J19
331870007005	CON;MINI DIN,7P,R/A,W/GROUND,351	J5
291000000802	CON;MINI PCI SOCKET,0.8MM,H4.0,S	J507

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9. Spare Parts List - 4

Part Number	Description	Location(S)
331810006044	CON;PHONE JACK,6P2C,H11.5,RJ11,T	J2
331910002006	CON;POWER JACK,2P,20VDC,5A,DIP	J23
331840010008	CON;STEREO JACK,10P,W/SPDIF,R/A,	J503
331840005007	CON;STEREO JACK,5P,R/A,W9.1,LGY2	J501,J502
331000008062	CON;USB,FM,H15.54,R/A,4P*2,SUYIN	J20
345673100028	CONDUCTIVE_TAPE;TP,COVER,8060	
345673100036	CONDUCTIVE-TAPE;KB,COVER,8060	
345673100037	CONDUCTIVE-TAPE;PANEL,CONN,8060	
342668200003	CONTACT PLATE;2,W4L20T0.15	
342503400004	CONTACT PLATE;W5L45T0.13,7170LI,	
342673100025	CONTACT PLATE;W5L46T0.13 ,2T,806	
342673100024	CONTACT PLATE;W5L62T0.13 ,1/3T,8	
342504300003	CONTACT PLATE;W5L63T0.13,8500	
342673100023	CONTACT PLATE;W5L80T0.13 ,1/5T,4	
342503400002	CONTACT PLATE;W5L9T0.13,7170LI,P	
313000150109	CORE;110OHM/100MH,15.0*14.0*23.0	
340676300001	COVER ASSY;8060B	
340673100021	COVER ASSY;DDR,8060	
340673100002	COVER ASSY;HINGE,8060	
340673100007	COVER ASSY;LCD,8060	
340673100022	COVER ASSY;MINIPCI,8060	
344673100008	COVER;BATT,8060	
344673100050	COVER-1;HDD,8060	
272615181401	CP;180P*4 ,8P,50V ,10%,0612,NPO,	CP504,CP505,CP506,CP507
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP501,CP503

Part Number	Description	Location(S)
227673100002	CUSHION;FRAME,FDD,AK BOX,8060	
227673100003	CUSHION;TOP/BTM,FDD,AK BOX,8060	
331660020004	DIMM SOCKET;DDR SODIMM 200P, CA0	J12
291000612004	DIMM SOCKET;DDR,200P,0.6MM,H4,SM	J504
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D504
288100054001	DIODE;BAT54,30V,200mA,SOT-23	D12,D14,D27,D502,D503
288100541002	DIODE;BAT54ALT1,COM. ANODE,SOT-2	PD2,PD501,PD502,PD503,PD504
288100541002	DIODE;BAT54ALT1,COM. ANODE,SOT-2	PD1
288100054002	DIODE;BAT54C,SCHOTTKY DIODE,SOT2	D19,D21,D515
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D516,PD10,PD506,PD507
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D1,D2
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D1
288100056003	DIODE;BAW56,70V,215mA,SOT-23	D508
288100084002	DIODE;BZX84C5V6,5.2~6V,350mA,SOT	ZD1,ZD2
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	D28,PD508
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD501
288100112003	DIODE;EC11FS2-TE12L,SCHOTTKY,200	D501,PD8
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD1,PD4,PD6,PD7,PD9
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D1
288100024003	DIODE;RLZ24B,ZENER,22.61~23.77,S	PD505
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	ZD5
288100018003	DIODE;UDZS18B,ZENER,18V,SOD-323,	ZD3,ZD4
344672300025	DUMMY CARD;PCMCIA,MANGUSTA	
523499990116	DVD ASSY OPTION;8060	
523430061904	DVD DRIVE; 8X,SDR-083,QUANTA	

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9. Spare Parts List - 5

Part Number	Description	Location(S)
523467310004	DVD ROM ASSY;8X,SDR-083,QSI,8060	
272601227501	EC;220U ,10V,M,6.3*7.7,-15+105',	C190,C206,C279,C285,C296
312278206152	EC;820U ,4V,+20%,10X10.5,FPCAP	PC1,PC5,PC6
227673100001	END CAP;L/R,8060	
227672300004	EPE PAD;K/B,MANGUSTA	
481676300002	F/W ASSY;KBD CTRL,8060B	U18
481676300001	F/W ASSY;SYS/VGA BIOS,8060B	U12
273000610025	FERRITE ARRAY;120OHM/100MHZ,ONLY	FA501
273000610025	FERRITE ARRAY;120OHM/100MHZ,ONLY	FA1
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L30,L4,L530
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,	L10,L11,L21,L23,L24,L31,L504,L
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,	L501,L502
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,	L16,L8
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L1,L12,L17,L2,L22,L27,L29,L50
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L1,L503,PL1,PL2
273000130015	FERRITE CHIP;220OHM/100MHZ,1608,	L518,L519,L520
273000150001	FERRITE CHIP;220OHM/100MHZ,2012,	L1
273000130006	FERRITE CHIP;600OHM/100MHZ,2A,1	L1,L10,L11,L12,L2,L3,L4,L5,L6,
332673100002	FFC;AUDIO,8060	
332673100003	FFC;TP,8060	
332673100004	FFC;TP,MB,8060	
346673100080	FILM;PANEL,330*224,8060	
345673100015	FILTER;INVERTER,LCD,8060	
288003602001	FIR;HSDL-3602-007,FRONT VIEW,10P	U26
245600010007	FLOW CARD;M/B,WHITE	

Part Number	Description	Location(S)
245600010016	FLOW CARD;SPS,GRAY	
245600010030	FLOW CARD;SPS,PINK,100MM*30MM,PR	
295000010044	FUSE;1.1A/6V,POLY SWITCH,1210,SM	F501,F502
295000010057	FUSE;228R,139C,5A/250V,SMT,PRC	
295000010126	FUSE;FAST,2A,63VDC,1206,SMT,PRC	F1
335152000062	FUSE;LR4-730,POLY SWITCH,PRC	
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF1,PF501,PF502
345673100027	GASKET;AUDIO,PCB,8060	
345673100024	GASKET;PCMCIA,MB,8060	
345673100043	GASKET;TVOUT,MB,8060	
451673100031	HDD ME KIT;8060	
340673100036	HEATSINK ASSY;CPU,8060	
343674900001	HEATSINK;NORTHBRIDGE,EN17	
342673100026	HEATSINK;VGA,8060	
341673100005	HINGE;LCD LEFT,8060	
341673100004	HINGE;LCD RIGHT,8060	
344673100045	HOLDER;PCMCIA,FCI-54922-22LOC,80	J13
340676300003	HOUSING ASSY;8060B	
340673100008	HOUSING ASSY;LCD,8060	
451676300001	HOUSING KIT;8060B	
344673100007	HOUSING;BATT,8060	
291000616803	IC SOCKET;BANIAS m-FCBGA478P, MO	U1
282574373004	IC;74AHC373,OCT D-TRAN,TSSOP,20P	U20
282574186002	IC;74AHCT1G86,SINGLE,XOR,SOT23,S	U21
282074338402	IC;74CBT D3384,10 BIT BUS SW,T SOP	U25

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Part Number	Description	Location(S)
282574164002	IC;74VHC164,SIPO REGISTER,TSSOP,	U501
284501032001	IC;ADM1032,TEMPERATURE MTR,SO8	U501,U6
286303301001	IC;ADP3301AR-5,.8%,REG.,SO,8P	U14
284500202005	IC;ALC202,AC97 CODEC,LQFP,48P,SM	U17
286308801006	IC;AME8801CEEV,VOL REG.,SOT23-5,	PU502
286308801009	IC;AME8801LEEV,VOL REG.,SOT25,5P	PU8
286002040001	IC;BQ2040,GAS GAUGE,SO,16P,SMT	U3
283466570001	IC;EEPROM,9346,64*16 BITS,SO8,SM	U508
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SM	U2
283410310002	IC;FLASH,512K*8-90,PLCC32,W29C04	
284582801044	IC;FW82801DBM,ICH4-M,BGA,421P	U507
284583437003	IC;H8/F3437S,KBD CTRL,TQFP,100P,	
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	PU507
283767630002	IC;HYB25D128323CL3.6,DDR SDRAM,4	U2,U5,U503,U504
284595081001	IC;ICS950810, CK408 CLOCK GEN, T	U506
286300811001	IC;IM811,MICROPWR VOL,SOT23-4	U23
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU19
284502996001	IC;LP2996,DDR,NS,PSOP8,SMT	PU1
286301772001	IC;MAX1772,PWM,QSOP,28P	PU21
286301858001	IC;MAX1858,PWM,QSOP,24P	PU5,PU505
286301858001	IC;MAX1858,PWM,QSOP,24P	PU504
286301907001	IC;MAX1907A,PWM CONTROLLER,40-QF	PU501
286301999001	IC;MAX1999,PWM,QSOP,28P	PU22
286133078001	IC;MC33078D,LOW NOISE OP AMP.,SO	U13
286301414001	IC;MM1414,PROTECTION,T SOP-20A,PR	U5

Part Number	Description	Location(S)
281307085001	IC;NC7SZ08P5,2-INPUT & GATE,SC70	U10,U513,U514
284500034002	IC;NV34M GPU,VGA CTRL,BGA701	U4
284500593001	IC;ODEM MCH-M mFCBGA 593p;PWR	U3
284500165001	IC;OZ165,AUDIO DI,TQFP,100P	U505
286300965001	IC;OZ965R,CCFL CTRL,TSSOP16,O2	U1
284587393002	IC;PC87393F,TQFP,100P	U515
284504510001	IC;PCI4510GHK,PC CARD,1394A CONT	U22
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U511
284500810002	IC;RTL8101L,LAN CONTROLLER,LQFP,	U9
286300812002	IC;S-812C,DECECTOR,SOT-89,PRC	U1
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ1
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ1
284591720001	IC;SPREAD MODULATING CLOCK GEN,I	U7
286100252001	IC;TPA0252,AUDIO AMP,2W,TSSOP,24	U510
286302211004	IC;TPS2211A,POWER INTERFACE SW,S	U15
273000990117	INDUCTOR;4.7UH,CDRH127,MULTI,SMT	PL24,PL30
273000990117	INDUCTOR;4.7UH,CDRH127,MULTI,SMT	PL502
273000990142	INDUCTOR;4.7UH,CDRH127B,SMT	PT1
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346673100008	INSULATOR;B,BATT,8060	
346503400502	INSULATOR;BATT ASSY,L22R9.2,8175	
346673100025	INSULATOR;BATT ASSY,L91.6W14MID8	
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BL	
346673100026	INSULATOR;BATT ASSY,POLY,W30L52,	
346673100027	INSULATOR;BATT ASSY,W13L20,BLAC,	

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Part Number	Description	Location(S)
346503400503	INSULATOR;BATT ASSY,W7L13,8175	
346673100040	INSULATOR;DCJACK,8060	
346673100028	INSULATOR;DDB,CMP,8060	
346673100023	INSULATOR;FOR 4 CELLS,8060	
346503200003	INSULATOR;FOR 5 CELLS,GRAMPUS	
346673100047	INSULATOR;INVERTER,8060	
346676300009	INSULATOR;KB,COVER,8060B	
346673100077	INSULATOR;KB,L-DOWN,8060	
346673100074	INSULATOR;KB,L-SIDE,8060	
346673100076	INSULATOR;KB,R-DOWN,8060	
346673100073	INSULATOR;KB,R-SIDE,8060	
346673100075	INSULATOR;KB,UP,8060	
346676300001	INSULATOR;MB,8060B	
346676300005	INSULATOR;MB,CAPACITOR,8060B	
346503900001	INSULATOR;PCB ASSY,W15L52,8575	
346673100014	INSULATOR;TP_PCB,8060	
346673100083	INSULATOR-1;T VOUT,8060	
531067310013	KBD ASSY;UI,8060	
531017240063	KBD;87,UI,3000160130,ZIPPY,8060	
451676300031	LABEL KIT;TCL W/NAMEPLATE,8060B	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000434	LABEL;25*6MM,COMMON	
242600000385	LABEL;27*10,LAN ID BAR CODE	
242600000378	LABEL;27*7MM,HI-TEMP 260°C	

Part Number	Description	Location(S)
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242673100002	LABEL;BATT,PANA,MSL,LI-ION,8060	
242600000433	LABEL;BLANK,11*5MM,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242669600005	LABEL;LOT NUMBER,RACE	
242674600010	LABEL;NVIDIA,CAIMAN	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000315	LABEL;RED ARROW HEAD,PRC	
242600000315	LABEL;RED ARROW HEAD,PRC	
441673100031	LCD ASSY;AU,WXGA,15.2",8060	
451673100051	LCD ME KIT;WXGA,15.2",8060	
413000020345	LCD;B152EW01,TFT,15.2",LVDS,WXGA	
294011200158	LED;BLUE,H=1.9,2.8X3.2MM,DDB-11,	D1
294011200155	LED;BLUE,H0.8,SF0603-B70140-30,S	D10,D11,D2,D3,D4,D5

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Part Number	Description	Location(S)
294011200161	LED;BLUE,H1.1,SF0805-B65140-38,S	D6
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190	LED1,2,3,4
294011200070	LED;RED/GREEN,19-22SRVGC/TR8,LED	LED5,6
416267630901	LT PF OPTION;WXGA,15.2",8060B	
416267630001	LT PF;AU,WXGA,15.2",8060B	
526267630015	LTXNX;8060B/W5AX/XXC/7UIX/L2D3A/	
346673100084	MYLAR;LCD,8060	
242676300002	NAMEPLATE;TCL,8060-B	
375102010002	NUT-HEX;M2X1.5,NIW	
461504100001	PACKING KIT;8060,BATT,LI	
461673100003	PACKING KIT;N-B,8060	
224670830002	PALLET;1250*1080*130,7521N	
221673150001	PARTITION;AK BOX,8060	
221503250001	PARTITION;BATTERY,GRAMPUS	
221600050113	PARTITION;FLAT,320MM*290MM,BC FL	
221673150004	PARTITION;PALLET,8060	
221503250002	PARTITION;TOP/BTM,BATTERY,GRAMPU	
412673100003	PCB ASSY;INVERTER board,MSL,for	
412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/	
316673100006	PCB;PWA- INVERTER BD,MSL,FOR 806	
316504100002	PCB;PWA-8060/BATT GAUGE BD	
316504100001	PCB;PWA-8060/BATT PROTECTION BD	
316673100004	PCB;PWA-8060/BUTTON BD	R01A
316676300003	PCB;PWA-8060-B/AUDIO BD	R0B
316676300002	PCB;PWA-8060-B/DD BD	R02

Part Number	Description	Location(S)
316676300001	PCB;PWA-8060-B/MOTHER BD	R01
222670820003	PE BAG;L560*W345,7521N	
222503220001	PE BUBBLE BAG;BATTERY,GRAMPUS	
340676300002	PLATE ASSY;CPU,8060B	
411673100004	PWA;PWA-8060,T/P BD,SMT	
411673100011	PWA;PWA-8060,T/P BD,T/U	
411504100003	PWA;PWA-8060/BATT GAUGE BD,LI	
411504100001	PWA;PWA-8060/BATT PROTECTION BD,	
411504100002	PWA;PWA-8060/BATT PROTECTION BD,	
411676300006	PWA;PWA-8060B,AUDIO BD	
411676300005	PWA;PWA-8060B,D/D BD,SMT	
411676300004	PWA;PWA-8060B,D/D BD,T/U	
411676300001	PWA;PWA-8060B,MOTHER BD	
411676300003	PWA;PWA-8060B,MOTHER BD,SMT	
411676300002	PWA;PWA-8060B,MOTHER BD,T/U	
411673100028	PWA;PWA-INVERTER BD,MSL FOR 8060	
411673100029	PWA;PWA-INVERTER BD,MSL FOR 8060	
332810000158	PWR CORD;250V10A,2P,BLK,CHINA,15	
271044027101	RES;002,2W,1%,2512,SMT	PR1,PR2
271046257101	RES;025 ,2W ,1% ,2512,SMT,PRC	R18,R18A
271045507101	RES;05 ,1W ,1% ,2512,SMT	PR17
271044061101	RES;06,2W,1%,2512,SMT,乾坤	PR36,PR37
271002000301	RES;0 ,1/10W,5% ,0805,SMT	R143,R186,R203,R204,R226,R275
271002000301	RES;0 ,1/10W,5% ,0805,SMT	PL3,PL4,PL5,PL6
271071000002	RES;0 ,1/16W,5% ,0603,SMT	L527,PR18,PR19,PR20,PR27,PR3

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Part Number	Description	Location(S)
271071000002	RES;0 ,1/16W,5% ,0603,SMT	PR1,R502
271071000002	RES;0 ,1/16W,5% ,0603,SMT	R508
271071010301	RES;1 ,1/16W,5% ,0603,SMT	PR23,PR24
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	PR517,R53,R54
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	R25,R26
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR21,PR22,PR52,PR6,R130,R154
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R9
271071102211	RES;10.2K,1/16W,1% ,0603,SMT	R5
271071101101	RES;100 ,1/16W,1% ,0603,SMT	PR30,R276,R303,R537,R643
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R37
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR34,PR35,PR50,PR518,PR523,P
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR507,PR511
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R16,R17
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R7
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR25,PR47,PR51,R158,R163,R22
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R1,R2
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R38,R44,R48
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R11,R15,R2,R8,R9
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR13,PR15,PR508,PR520,PR521,
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR3,PR505,PR506
271071103101	RES;10K ,1/16W,1% ,0603,SMT	R18
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR3,PR4,PR505,PR510,PR527,R1
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R507
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R3,R4
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R622,R628

Part Number	Description	Location(S)
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	PR38,PR39
271071131101	RES;130 ,1/16W,1% ,0603,SMT	R582
271071150301	RES;15 ,1/16W,5% ,0603,SMT	R36,R37,R39,R40,R42,R45,R46,R4
271071154102	RES;15.4K ,1/16W,1% ,0603,SMT	PR560
271071154102	RES;15.4K ,1/16W,1% ,0603,SMT	PR10
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R187,R188,R23,R48,R51,R521,R5
271071154101	RES;150K ,1/16W,1% ,0603,SMT	R1
271071153101	RES;15K ,1/16W,1% ,0603,SMT	R3,R4
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R175
271071164301	RES;160K ,1/16W,5% ,0603,SMT	R42
271071182213	RES;18.2,1/16W,1% ,0603,SMT	R649
271071184301	RES;180K ,1/16W,5% ,0603,SMT	R166
271002102301	RES;1K ,1/10W,5% ,0805,SMT	PR62
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR44,PR46,PR48,PR511,PR516,P
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR6
271071102102	RES;1K ,1/16W,1% ,0603,SMT	R8,R15,R19
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R114,R126,R128,R165,R172,R176
271071102302	RES;1K ,1/16W,5% ,0603,SMT	PR8
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R35,R39,R43
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR549,PR569
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R13
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR41,PR43,PR45,PR5,PR501,PR5
271071222102	RES;2.2K ,1/16W,1% ,0603,SMT	PR522
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R581,R583,R585,R617,R618,R644
271071225301	RES;2.2M,1/16W,5% ,0603,SMT	R34,R36

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Part Number	Description	Location(S)
271034278301	RES;2.7 ,1/2W ,5% ,2010,SMT	R695
271071272101	RES;2.7K ,1/16W,1% ,0603,SMT	PR4
271071272301	RES;2.7K ,1/16W,5% ,0603,SMT	R221,R295,R296
271071201101	RES;200 ,1/16W,1% ,0603,SMT	PR513,PR514
271071201301	RES;200 ,1/16W,5% ,0603,SMT	R14,R17
271071204101	RES;200K ,1/16W,1% ,0603,SMT	R40
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR543
271071203101	RES;20K ,1/16W,1% ,0603,SMT	R2
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R299,R655,R656,R672,R673,R68,
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R241,R242,R262,R263,R264,R279
271071223302	RES;22K ,1/16W,5% ,0603,SMT	R217
271071244301	RES;240K ,1/16W,5% ,0603,SMT	R41
271071244102	RES;240K,1/16W,1%,0603,SMT	PR537
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R25
271071274811	RES;27.4 ,1/16W,1% ,0603,SMT	R31,R38,R505,R534
271071202102	RES;2K ,1/16W,1% ,0603,SMT	R515
271071205101	RES;2M ,1/16W,1% ,0603,SMT	R11
271071348111	RES;3.48K,1/16W,1%,0603,SMT	PR12
271071301812	RES;30.1,1/16W,1%,0603,SMT	R56
271071301011	RES;301 ,1/16W,1% ,0603,SMT	R525,R536
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR555
271071303101	RES;30K ,1/16W,1% ,0603,SMT	PR49,PR525,PR535
271071303101	RES;30K ,1/16W,1% ,0603,SMT	PR509
271071330302	RES;33 ,1/16W,5% ,0603,SMT	PR28,PR550,R122,R123,R124,R12
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R502

Part Number	Description	Location(S)
271071334301	RES;330K ,1/16W,5% ,0603,SMT	R216
271071334102	RES;330K,1/16W,1%,0603,SMT	PR5
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R554,R679,R684
271072365811	RES;36.5 ,1/10W,1% ,0603,SMT	R182,R52,R528
271071390302	RES;39 ,1/16W,5% ,0603,SMT	R21
271002478301	RES;4.7 ,1/10W,5% ,0805,SMT	PR14,PR551,PR7
271002478301	RES;4.7 ,1/10W,5% ,0805,SMT	PR508
271071478101	RES;4.7 ,1/16W,1% ,0603,SMT	PR10,PR33,PR533,PR536,PR554,
271071478301	RES;4.7 ,1/16W,5% ,0603,SMT	PR503,PR504
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR545,PR546
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR528,PR548,R214,R271,R306,R
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R501,R506
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR524,PR532,PR538,PR542
271071402311	RES;402K ,1/16W,1% ,0603,SMT	PR40
271071412211	RES;41.2K,1/16W,1% ,0603,SMT	PR16
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	PR26
271071433301	RES;43K ,1/16W,5% ,0603,SMT	R280
271071471101	RES;470 ,1/16W,1% ,0603,SMT	R21,23,27
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R547
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R10,R11,R2,R3,R4,R9
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R510
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R1
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R29,R526
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR2,PR501,PR7
271071475011	RES;475 ,1/16W,1% ,0603,SMT	R121

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Part Number	Description	Location(S)
271071475311	RES;475K ,1/16W,1% ,0603,SMT	PR11,PR32,PR557,PR558
271071473101	RES;47K ,1/16W,1% ,0603,SMT	PR509,PR53,PR57,PR60
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R119,R120,R129,R138,R144,R210
271071487211	RES;48.7K,1/16W,1% ,0603,SMT	R7
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R141,R142,R201,R202,R510,R511
271071499211	RES;49.9K,1/16W,1% ,0603,SMT	PR29
271071512101	RES;5.1K ,1/16W,1% ,0603,SMT	PR8,R225,R240
271071512101	RES;5.1K ,1/16W,1% ,0603,SMT	PR510,PR9
271002515302	RES;5.1M ,1/8W ,5% ,0805,SMT,PRC	R10
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R101,R106,R108,R135,R35,R614,
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R45
271071510301	RES;51 ,1/16W,5% ,0603,SMT	R14,R17,R18,R19,R506
271071513301	RES;51K ,1/16W,5% ,0603,SMT	R667,R668
271071549811	RES;54.9 ,1/16W,1% ,0603,SMT	R30,R504
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R155,R156,R160,R27,R5,R501
271071562811	RES;56.2 ,1/16W,1% ,0603,SMT	R235,R236,R253,R257,R258,R259
271071561101	RES;560 ,1/16W,1% ,0603,SMT	R22,24,28
271071634111	RES;6.34K,1/16W,1% ,0603,SMT	R266
271071682301	RES;6.8K ,1/16W,5% ,0603,SMT	R215
271071698101	RES;6.98K,1/16W,1%,0603,SMT	PR564
271071623101	RES;62K ,1/16W,1% ,0603,SMT	PR507
271071631101	RES;63.4,1/16W,1% ,0603,SMT	R598
271071680101	RES;68 ,1/16W,1% ,0603,SMT	R44,R544,R560,R566
271071681101	RES;680 ,1/16W,1% ,0603,SMT	R1
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R24

Part Number	Description	Location(S)
271071683101	RES;68K ,1/16W,1% ,0603,SMT	R12
271071683301	RES;68K ,1/16W,5% ,0603,SMT	R219
271071698311	RES;698K ,1/16W,1% ,0603,SMT	R5
271071750302	RES;75 ,1/16W,5% ,0603,SMT	R245,R250,R707,R708
271071751101	RES;750 ,1/16W,1% ,0603,SMT	PR515,PR519
271071822102	RES;8.2K ,1/16W,1% ,0603,SMT	PR502
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R161,R638
271071823102	RES;82K,1/16W,1%,0603,SMT	PR512
271071887211	RES;88.7K,1/16W,1% ,0603,SMT	R6
271071909011	RES;909 ,1/16W,1% ,0603,SMT	R14
451673100001	ROM ME KIT;8060	
271611100301	RP;10*4 ,8P ,1/16W,5% ,0612,SMT	RP10,RP3,RP4,RP9
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP11,RP12,RP13,RP14,RP15,RP16
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP1,RP527
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP2
271611222301	RP;2.2K*4,8P ,1/16W,5% ,0612,SMT	RP505,RP507,RP523,RP525
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP504,RP506,RP522,RP524,RP526
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP530
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT	RP532
271621473301	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	RP18,RP529
271571560302	RP;56*8 ,16P,1/16W,5% ,1606,SMT	RP508,RP509,RP510,RP511,RP512
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP501,RP502
271621822302	RP;8.2K*8,10P,1/32W,5% ,1206,SMT	RP17,RP526,RP528
345673100040	RUBBER FOOT;8060	
345673100005	RUBBER;LCD DOWN,8060	

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Part Number	Description	Location(S)
345673100006	RUBBER;LCD UP,8060	
345671200002	RUBBER;MIDDLE,LCD,8170	
565167630001	SW;CD ROM,SYSTEM DRIVER,8060B	
565180626001	SW;CD*1,DVD,WIN-DVD,INTERVIDEO	
371102030303	SCREW;M2L3,K-HEAD(+),NIW/NLK	
340673100031	SHIELDIND ASSY-1;HDD,8060	
340673100034	SHIELDING ASSY-1;IO,8060	
333020000003	SHRINK TUBE;600V,105°C,D0.8*5MM,	
333050000107	SHRINK TUBE;UL,600V,105°C,ID2.5*	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
365350000003	SOLDER WIRE;0.8MM,SN43/PB43/BI14	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010005	SOLDER WIRE;63/37,0.8,NA,N/C,PRC	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,	
370102631202	SPC-SCREW;M2.6L6,K-HD,NIW/NLK	
370102631202	SPC-SCREW;M2.6L6,K-HD,NIW/NLK	
370102010201	SPC-SCREW;M2L2,NIW,K-HD,t=0.8,NL	
370102010253	SPC-SCREW;M2L2.5,NIW/NLK,HD07	
370102020301	SPC-SCREW;M2L3,NIW,K-HEAD	
370102020301	SPC-SCREW;M2L3,NIW,K-HEAD	
370102020301	SPC-SCREW;M2L3,NIW,K-HEAD	

Part Number	Description	Location(S)
370102010404	SPC-SCREW;M2L4,K-HD,NIB	
370102010405	SPC-SCREW;M2L4,NIW,K-HD(+),NYLOK	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
340676300006	SPEAKER ASSY;L,2W,8060B	
340676300005	SPEAKER ASSY;R,2W,8060B	
346676300006	SPONGE;DDB,SWITCH,8060B	
346673100086	SPONGE;KB,L,COVER,8060	
346673100087	SPONGE;KB,R,COVER,8060	
346676300007	SPONGE;THERMAL,MB,CPU,8060B	
346676300008	SPONGE;THERMAL,MB,HDD,8060B	
346673100068	SPONGE3;THERMAL,MB,8060	
341673100011	SPRING SCREW;CPU HEAT SINK,8060	
342673100014	ST AND OFF;M2L8.3,CASHI,8060	
342673100018	ST AND OFF;MDC,8060	
337040100005	SW;PUSH BUTTON,SPST,12V50MA,RA,H	SW501,SW502,SW503,SW504,SW
297040100002	SW;PUSH BUTTON,SPST,4P,15V/20mA,	SW1,SW2
297040100002	SW;PUSH BUTTON,SPST,4P,15V/20mA,	SW1
225000020002	TAPE;1/2",2 ADHESIVE FACE,20YARD	
622200000008	TAPE;CARTON,2.5"W,30M/RL,PRC	
225600000054	TAPE;INSULATING,POLYESTER FILM,1	
346673100054	THERMAL PAD,NB,8060	
310111103011	THERMISTOR;10K,1%,RA,DISK,103AT-	T1
442673100051	TOUCH PAD MODULE;TM41P-311,SYNAP	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	PQ3,PQ4,PQ501,PQ503,PQ6,Q50
628820014401	TRANS;DTA144EKA,PNP,100MA,50V,SO	Q6,Q7

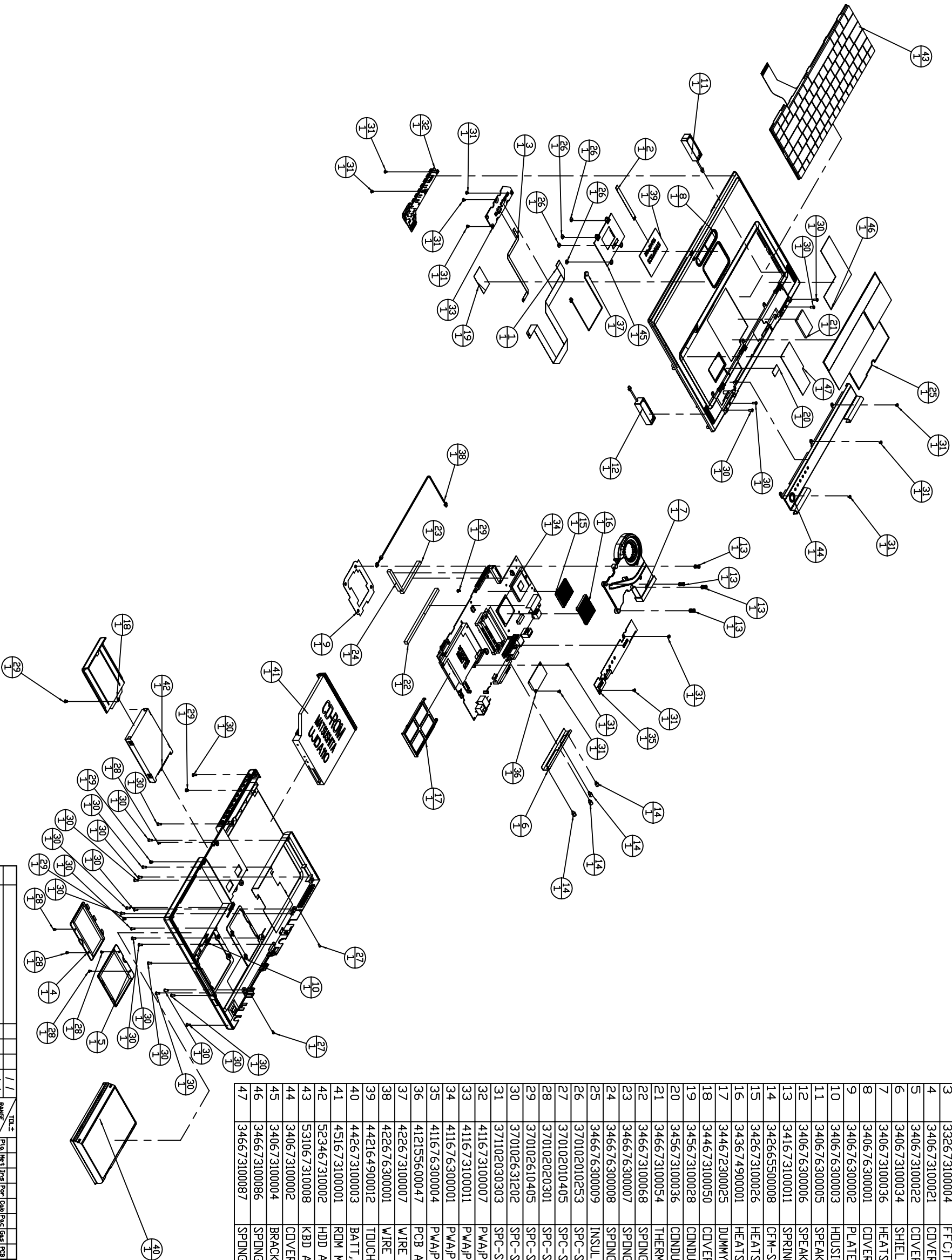
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Part Number	Description	Location(S)
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q2,Q3,Q4,Q5,Q504,Q507,Q510,Q
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q502
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q7
288203906002	TRANS;MMBT3906L,40V,200mA,SOT23,	Q1
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	PQ2
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	PQ2,Q1
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q501
288202303001	TRANS;SI2303DS,P-MOSFET,SOT-23	PQ502,Q9
288202304001	TRANS;SI2304DS,N-MOSFET,SOT-23	Q10
288104362001	TRANS;SI4362DY,N-HOSFET,S08	PU10,PU503
288104362001	TRANS;SI4362DY,N-HOSFET,S08	PU3,PU503
288204425002	TRANS;SI4425DY,PMOS,8.5A/30V,0.0	Q2,Q2A,Q3,Q3A
288204532001	TRANS;SI4532DY,N&P-MOSFET,S08,PR	U2
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU11,PU12,PU14,PU15,PU20,PU
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU2,PU501
288204816001	TRANS;SI4816DY,2 N-MOSFET,30V,SO	PU6,PU7
288204816001	TRANS;SI4816DY,2 N-MOSFET,30V,SO	PU4
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PU13,PU16,PU23,PU504
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	PU17,PU18
288204892001	TRANS;SI4892DY,N-MOSFET,S08	PU9
288204892001	TRANS;SI4892DY,N-MOSFET,S08	PU502
288217886001	TRANS;SI7886DP,N-MOSFET,S08	PU1,PU2
288217888001	TRANS;SI7888DP,N-MOSFET,S08	PU3,PU4
288208107001	TRANS;TPC8107,13A/30V,P-MOSFET,S	PQ5,PU24
273001050022	TRANSFORMER;10/100 BASE,PH163112	U11

Part Number	Description	Location(S)
373101712351	T-SCREW;B,M1.7,L2.35,K-HD,2,NIB	
270140000003	VARISTOR;280V,5.6X3.8MM,TVB280-0	S1
421666200009	WIRE ASSY;BATTERY BIOS,NV	
422673100004	WIRE ASSY;INVERTOR,LCD,8060	
422676300001	WIRE ASSY;MDC,8060B	
422673100007	WIRE ASSY;MIC,8060	
422673100001	WIRE LCD ASSY;LCD,8060	
332110020111	WIRE;#20,UL1007,120MM,RED,YIYI;P	
332110020109	WIRE;#20,UL1007,65MM,BLACK,YIYI;	
332110020094	WIRE;#20,UL1007,65MM,RED,YIYI;PW	
332110026130	WIRE;#26,UL1007,45MM,BLACK,YIYI;	
332110026128	WIRE;#26,UL1007,65MM,YELLOW,YIYI	
332110026125	WIRE;#26,UL1007,81MM,WHITE,YIYI;	
273001050118	XSFORMER;CI8.5,SIT16260-0839B,16	T1
274011431408	XTAL;14.318M,50PPM,32PF,7*5,4P,S	X2
274011600408	XTAL;16MHZ,16PF,50PPM,8*4.5,2P	X7
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	X5,X6
274012500401	XTAL;25MHZ,30PPM,18PF,4P,SMT	X4
274012700401	XTAL;27MHZ,20PPM,16PF,7*5,4P,SMT	X1
274013276114	XTAL;32.768KHZ,10PPM,12.5PF	X3
274010800401	XTAL;8MHZ,30PPM,16PF,7*5,4P,SMT	X501
		P/N:526267630015

ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	332673100002	FFC, AUDIO, 8060	1	PART	
2	332673100003	FFC, ITP, 8060	1	PART	
3	332673100004	FFC, ITP, MB, 8060	1	PART	
4	340673100021	COVER ASSY, DDR, 8060	1	ASSEMBLY	
5	340673100022	COVER ASSY, MINIPCT, 8060	1	ASSEMBLY	
6	340673100034	SHIELDING ASSY-1, ID, 8060	1	ASSEMBLY	
7	340673100036	HEAT SINK ASSY, CPU, 8060	1	ASSEMBLY	
8	340676300001	COVER ASSY, 8060B	1	ASSEMBLY	
9	340676300002	PLATE ASSY, CPU, 8060B	1	ASSEMBLY	
10	340676300003	HOUSING ASSY, 8060B	1	ASSEMBLY	
11	340676300005	SPEAKER ASSY, L, 2W, 8060B	1	ASSEMBLY	
12	340676300006	SPEAKER ASSY, R, 2W, 8060B	1	ASSEMBLY	
13	341673100011	SPRING SCREW, CPU HEAT SINK, 8060	4	ASSEMBLY	
14	342665500008	CFM-SUITS, S-STANDOFF	4	PART	
15	342673100026	HEAT SINK, VGA, 8060	1	PART	
16	343674900001	HEAT SINK, MDRTH BRIDGE, EN17	1	PART	
17	344672300025	DUMMY CARD, PCMCIA, MANGUSTA	1	PART	
18	344673100050	COVER-1, HDD, 8060	1	PART	
19	345673100028	CONDUCTIVE TAPE, ITP COVER, 8060	1	PART	
20	345673100036	CONDUCTIVE TAPE, ITP COVER, 8060	1	PART	
21	346673100054	THERMAL PAD, NB, 8060	1	PART	
22	346673100068	SPDNGE, 3, THERMAL, MB, 8060	1	PART	
23	346676300007	SPDNGE, THERMAL, MB, CPU, 8060B	1	PART	
24	346676300008	SPDNGE, THERMAL, MB, HDD, 8060B	1	PART	
25	346676300009	INSUL. ATDR, KB, COVER, 8060B	1	ASSEMBLY	
26	370102010253	SPC-SCREW, M2.5, NIW, NV	4	PART	
27	370102010405	SPC-SCREW, M2.4, NIW, K-HD(+)-NLK	2	PART	
28	370102020301	SPC-SCREW, M2.3, NIW, K-HD	5	PART	
29	370102610405	SPC-SCREW, M2.6, K-HD, NIW, NLK	5	PART	
30	370102631202	SPC-SCREW, M2.6, K-HD, NIW, NLK	21	PART	
31	371102030303	SPC-SCREW, M2.3 K-HEAD, NIW	12	PART	
32	411673100007	PVA/PWA-8060, AUDIO BD	1	ASSEMBLY	
33	411673100011	PVA/PWA-8060, T/P BD, T/U	1	ASSEMBLY	
34	411676300001	PVA/PWA-8060B, MOTHER BD, T/U	1	ASSEMBLY	
35	411676300004	PVA/PWA-8060B, D/D BD, T/U	1	ASSEMBLY	
36	412155600047	PCB ASSY, MDM, 56K, UNIV, F-PACK, WD/	1	ASSEMBLY	
37	422673100007	WIRE ASSY, MIC, 8060	1	ASSEMBLY	
38	422676300001	WIRE ASSY, MDC, 8060B	1	ASSEMBLY	
39	442164900012	TOUCH PAD MODULE, TM41P-311, SYNAP	1	PART	
40	442673100003	BATT ASSY, 11.1V/6AH, LI-PANASONIC	1	ASSEMBLY	
41	451673100001	ROM ME KIT, 8060	1	ASSEMBLY	
42	523467310002	HDD ASSY, 30G, FUJITSU MHR2030AT, 8	1	ASSEMBLY	
43	531067310008	KBD ASSY, IGR, 8060	1	ASSEMBLY	
44	340673100002	COVER ASSY, HINGE, 8060	1	ASSEMBLY	
45	340673100004	BRACKET ASSY, ITP, 8060	1	ASSEMBLY	
46	346673100086	SPDNGE, KB, L, COVER, 8060	1	PART	
47	346673100087	SPDNGE, KB, R, COVER, 8060	1	PART	



ITEM	CONTENTS OF CHANGE	REV	CHK	APPV	W/D	DATE	SCALE	UNIT	REMARK
1	1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4	4	4
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46	46	46	46	46	46	46	46	46	46
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DRAW	DESIGN	CHECK	ISSUED

PCB	PCBA
R0A	0.1
R0B	0.2
R0C	0.3
R01	1.0

POWER STATES

STATE	SIGNAL	VOTAGE	S0	S1	S3	S4	S5
-SUSA	-	HIGH	LOW	LOW	LOW	LOW	LOW
-SUSB	-	HIGH	LOW	LOW	LOW	LOW	LOW
-SUSC	-	HIGH	LOW	LOW	LOW	LOW	LOW
DVMAIN	+19V	0	0	0	0	0	0
DBATT	+12.6V	0	0	0	0	0	0
RTC_VCC	+3.3V	0	0	0	0	0	0
CPU_CORE	+0.956V~+1.468V	0	0	X	X	X	X
+1.35VS	+1.35V	0	0	X	X	X	X
+1.8VS	+1.8V	0	0	X	X	X	X
DDR_2.5V	+2.5V	0	0	0	X	X	X
VGA_MEM2.5	+2.5V	0	0	X	X	X	X
+3VS	+3.3V	0	0	X	X	X	X
+3V	+3.3V	0	0	0	X	X	X
+5VS	+5V	0	0	X	X	X	X
+5V	+5V	0	0	0	X	X	X
+5VA	+5V	0	0	0	0	0	0
+12VS	+12V	0	0	X	X	X	X
+12V	+12V	0	0	0	X	X	X
+5V_CD	+5V	0	0	0	0	0	0/X byADJ_BTN
+5VAS	+5V	0	0	0	0	X	X
+1.5V	+1.5V	0	0	0	X	X	X
+1.5VS	+1.5V	0	0	X	X	X	X
REF_1.25V	+1.25V	0	0	X	X	X	X
+VCCP	+1.05V	0	0	X	X	X	X
+1.2VS	+1.2V	0	0	X	X	X	X
+2.8VS	+2.8V	0	0	X	X	X	X

IDSEL

IDSEL	CHIP
AD11	
AD17	MINIPCI
AD18	LAN RTL8101L
AD19	PCMCIA/IEEE1394
AD21	

PCIINT

PCIINT	CHIP
INTA	NV18M-PRO
INTB	MINIPCI
INTC	PCI4510
INTD	LAN RTL8101L
INTE	MINIPCI
INTF	PCI4510
INTG	OZ165
INTH	PULL -HI

BUS MASTER

REQ/GNT	CHIP
-REQ0/-GNT0	PCMCIA 4510
-REQ1/-GNT1	PULL -HI
-REQ2/-GNT2	LAN RTL8101L
-REQ3/-GNT3	MINIPCI
-REQ4/-GNT4	PULL -HI

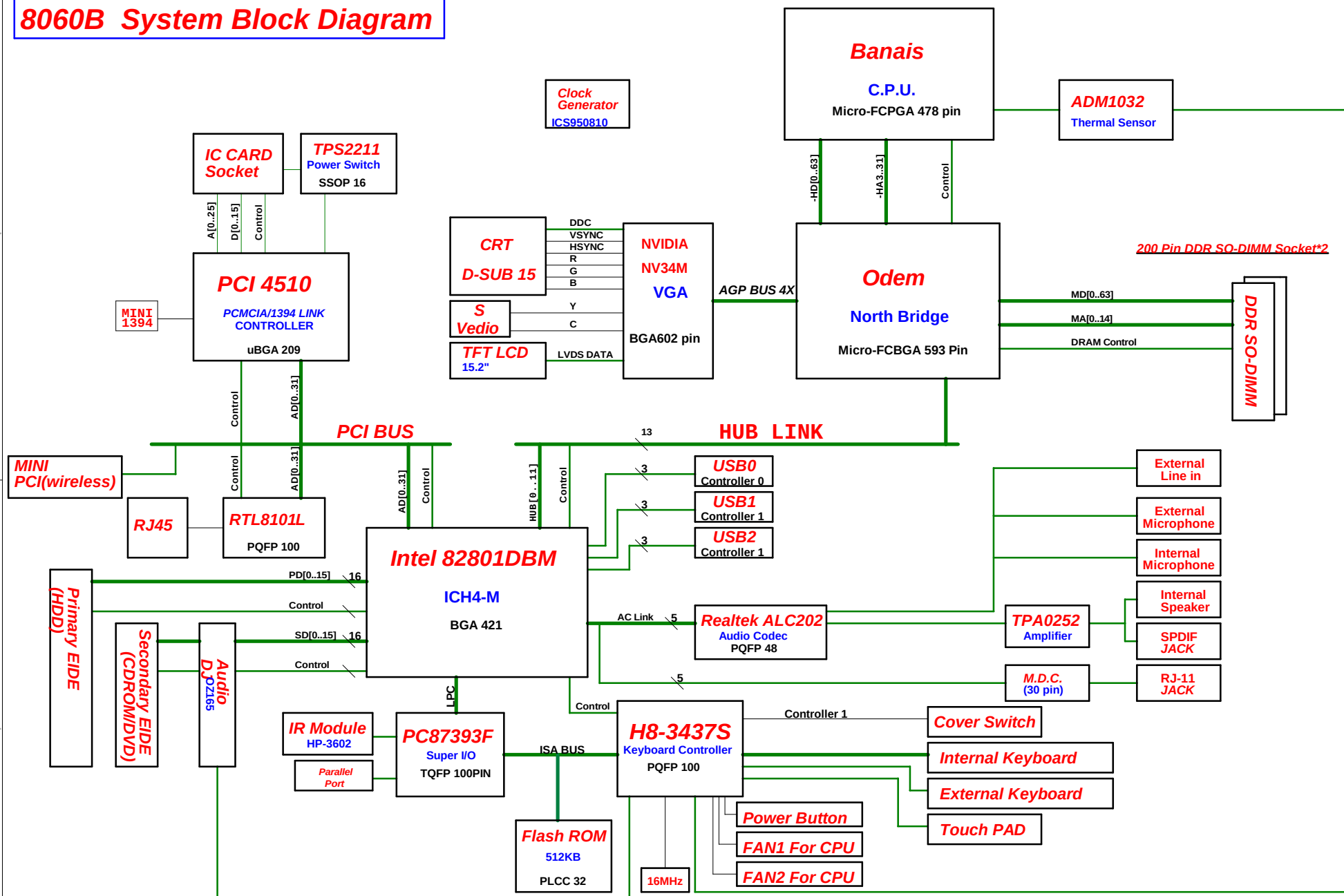
1	CORP
2	GND
3	IN-1
4	IN-2
5	POWER
6	IN-3
7	GND
8	SOLDER

* OPTION(NO LINK)

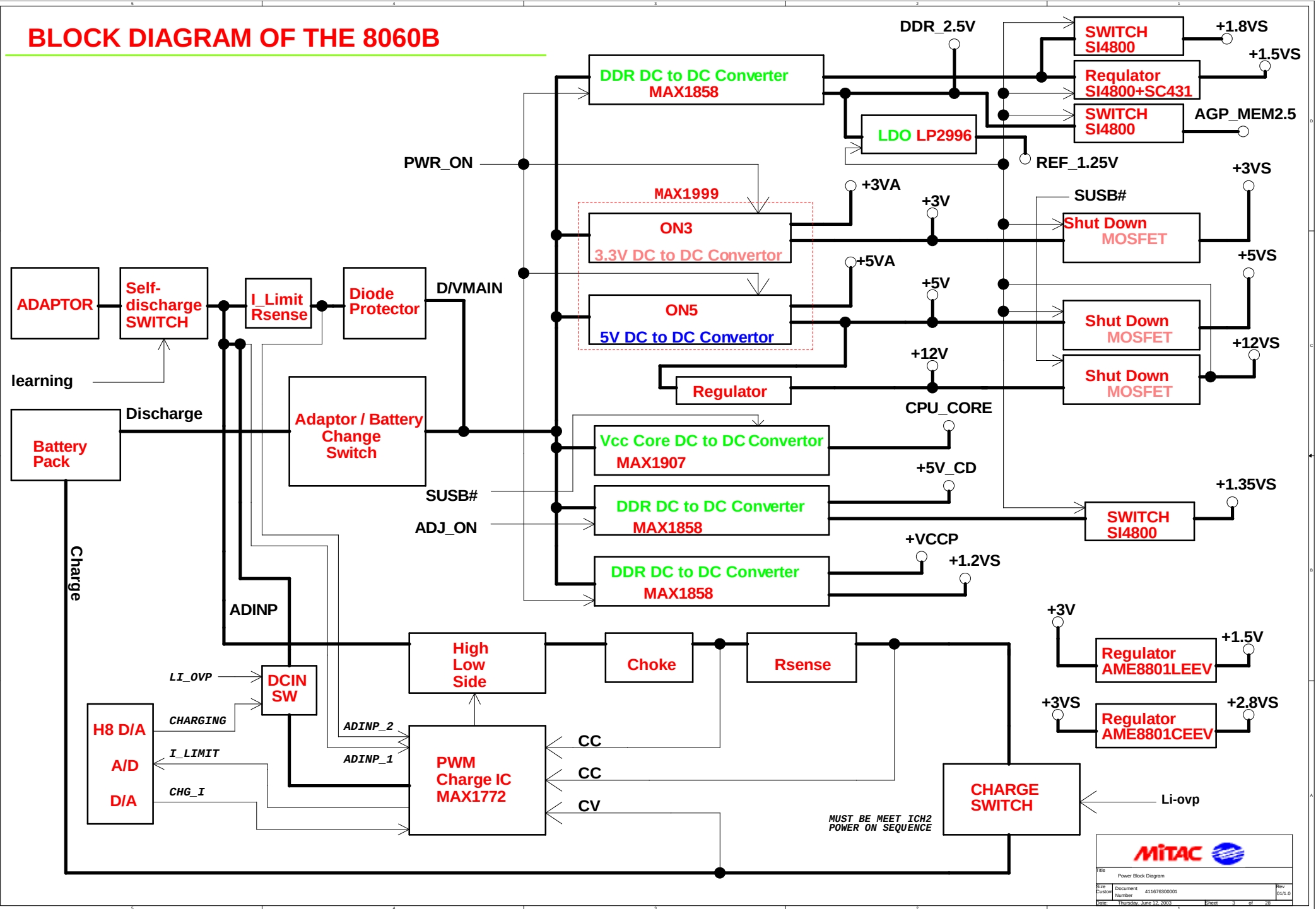
RTC	ICH3M	4uA
+VCCP	Banias ODEM	2.5A 2.4A
+1.2VS	ODEM	1.65A
REF_1.25V	DDR	2.4A
+1.35VS(+1.3VS)	MV34M	7A-8A
+1.5VS	ODEM NV18M PRO ICH4M	370mA 550mA 67.5mA
+1.5V	ICH4M	67.5mA
CPU_CORE	BANIAS	21A
+1.8VS	BANIAS ODEM ICH4	120mA 200mA 132mA
DDR_2.5V	DDR	6A
VGA_MEM2.5	NV18-M PRO	3A
+3V	ICH4M RTL8101L PCI4510 PCMCIA CARD	520mA 20mA 330mA 60mA
+3VS	ICH4M CLOCK NV18-M PRO LCD	120mA 180mA 0.6A 50mA 1.5A
+5V	USB*3 PCMCIA MINIPCI CARD	1.5A 1A 0.3A
+5VS	IDE ALCC200 MODEM	1A 0.5A 0.5A
+5VA	H8	40mA
+5V_CD	AUDIO AMP CD_ROM	1.2A 1.8A

MITAC	
File	Cover Sheet
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Docu	Document
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8060B System Block Diagram



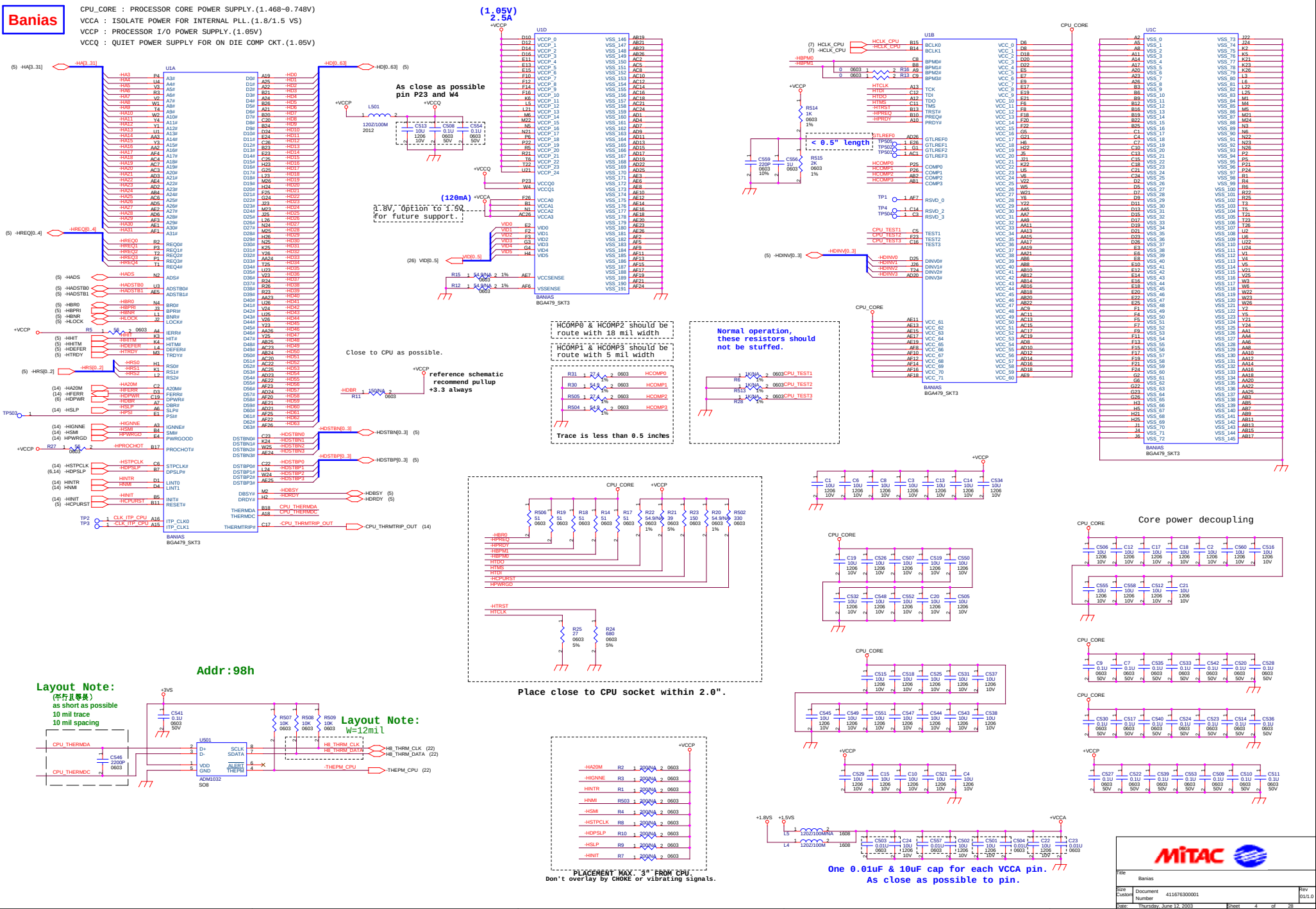
BLOCK DIAGRAM OF THE 8060B



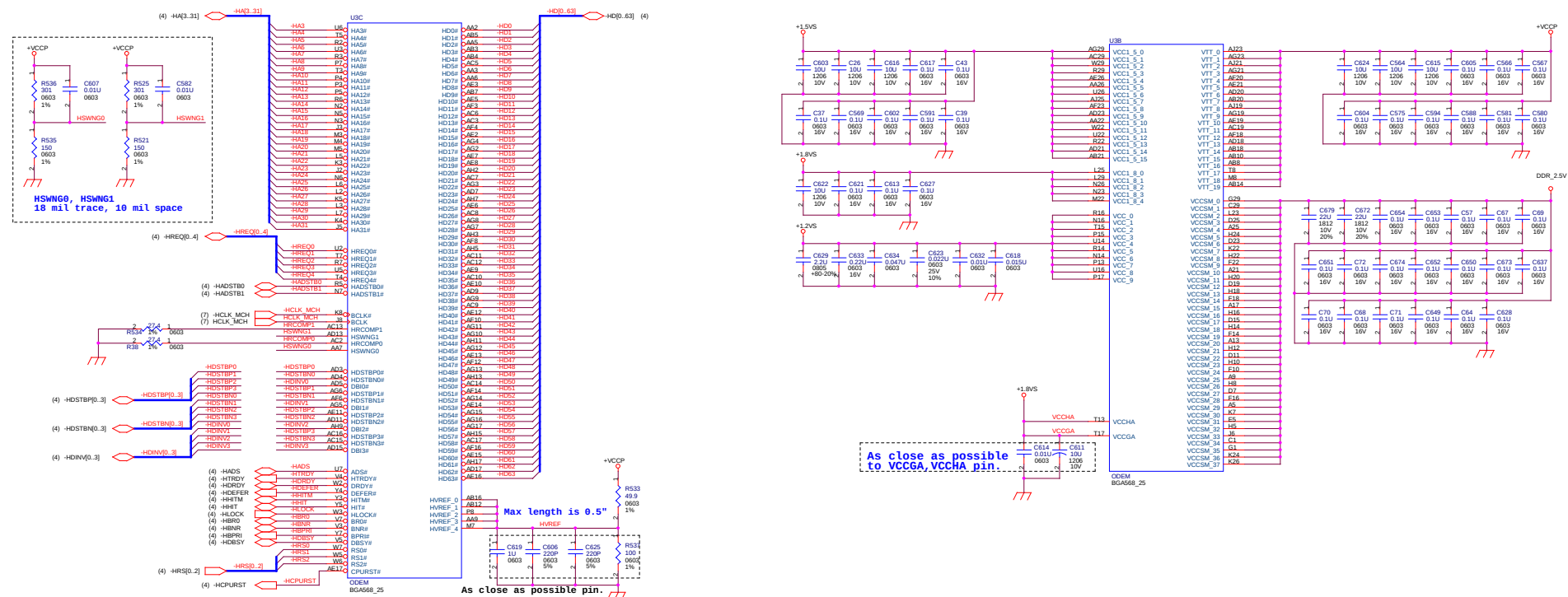
Mitsubishi		
Power Block Diagram		
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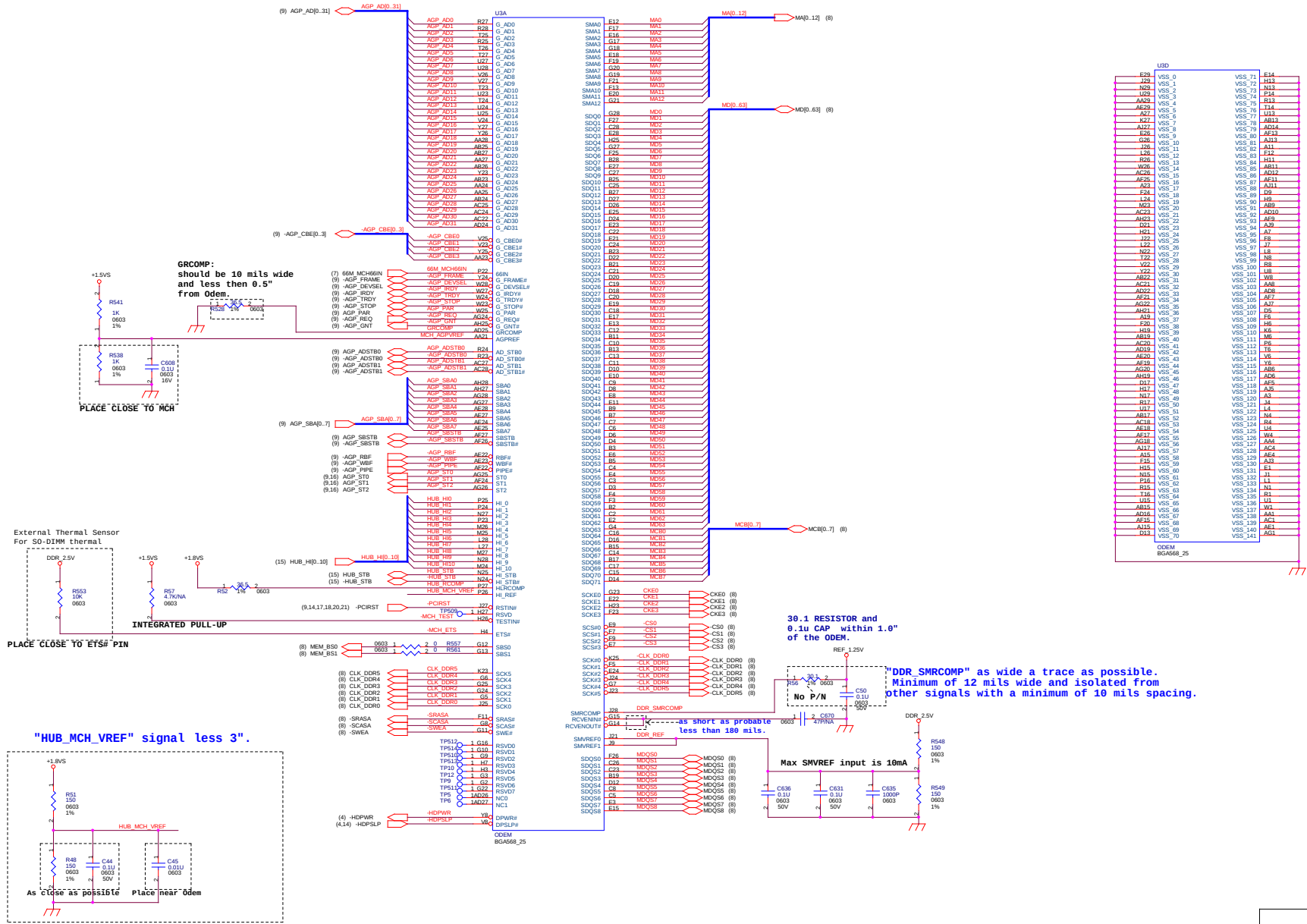
Banias

CPU_CORE : PROCESSOR CORE POWER SUPPLY.(1.468-0.748V)
VCCA : ISOLATE POWER FOR INTERNAL PLL.(1.8/1.5 VS)
VCCP : PROCESSOR I/O POWER SUPPLY.(1.05V)
VCCQ : QUIET POWER SUPPLY FOR ON DIE COMP CKT.(1.05V)

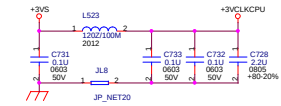


Odem

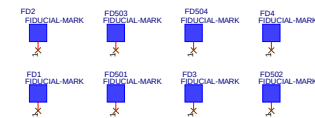
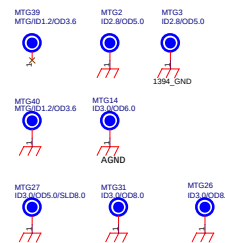
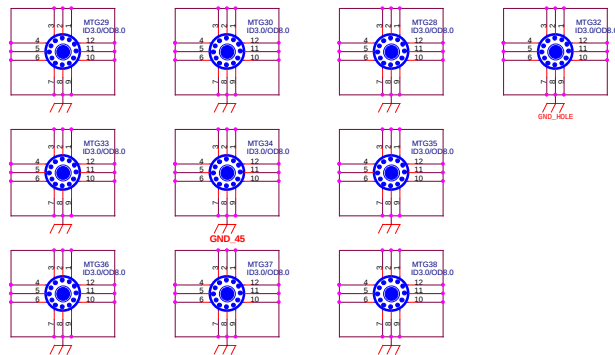
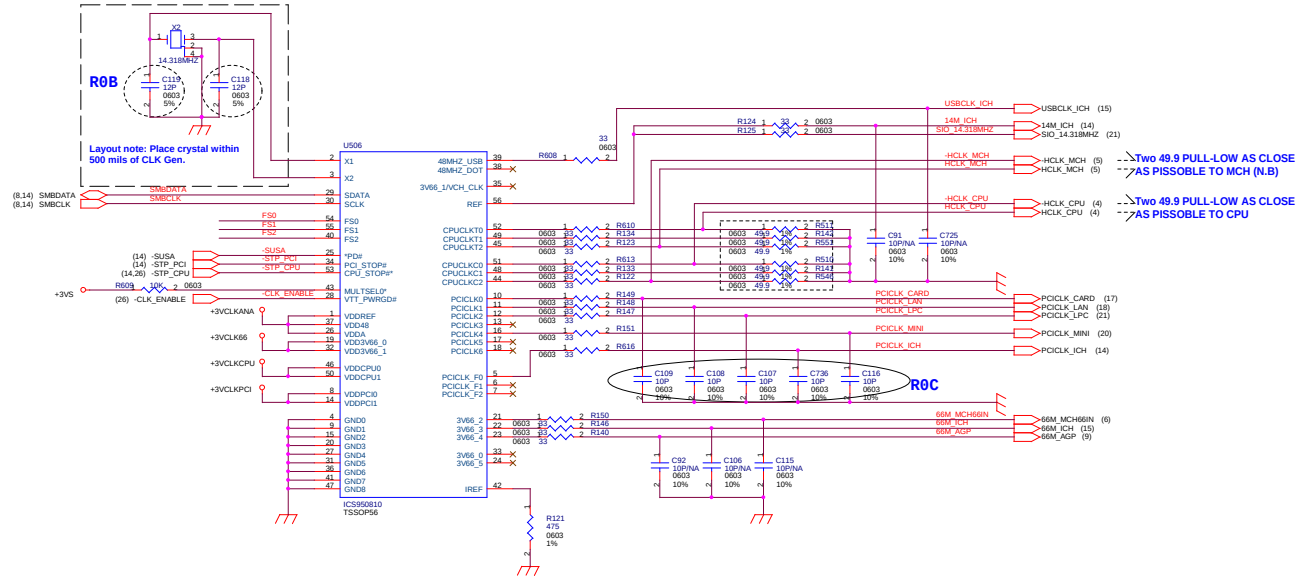
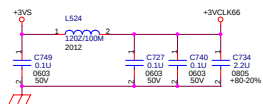
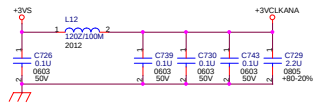
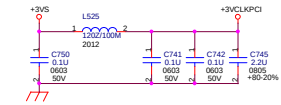




CLOCK GENERATOR



FS2	FS1	FS0	CPULCK
0	0	1	100MHZ
0	1	1	133MHZ



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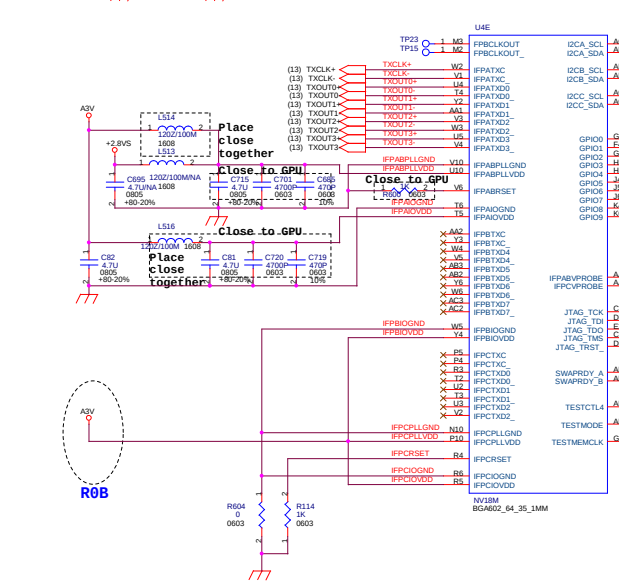
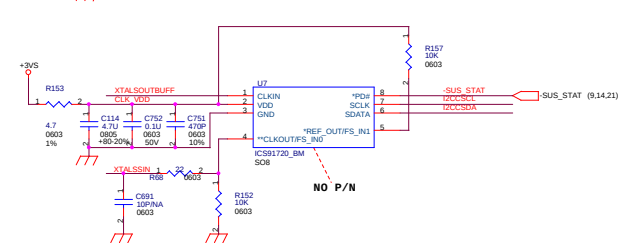
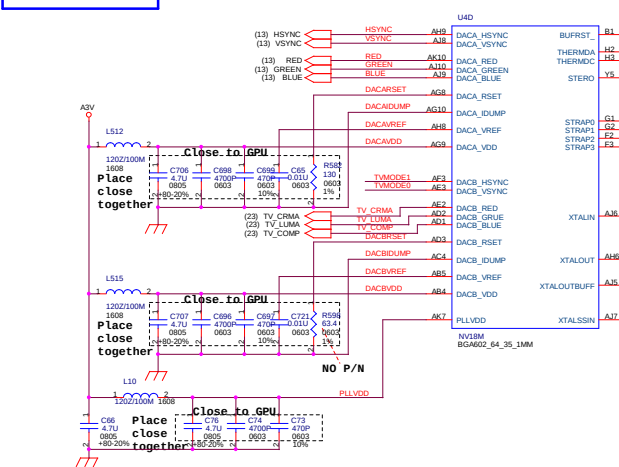
DDR SO-DIMM Module



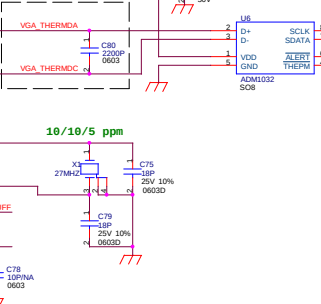
NV18M/NV31



NV18M/NV31



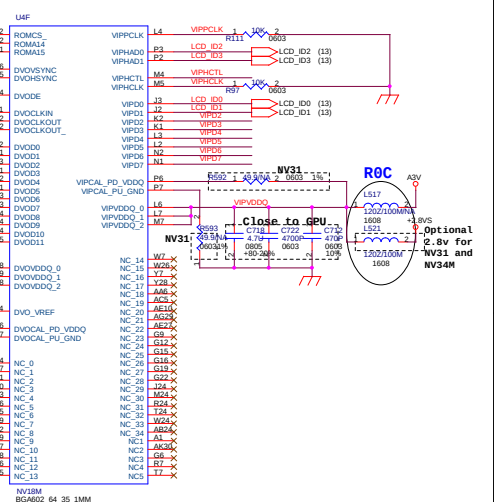
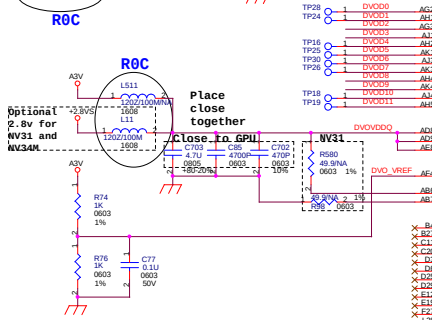
Layout Note:
(平行且等長)
as short as possible
10 mil trace
10 mil spacing



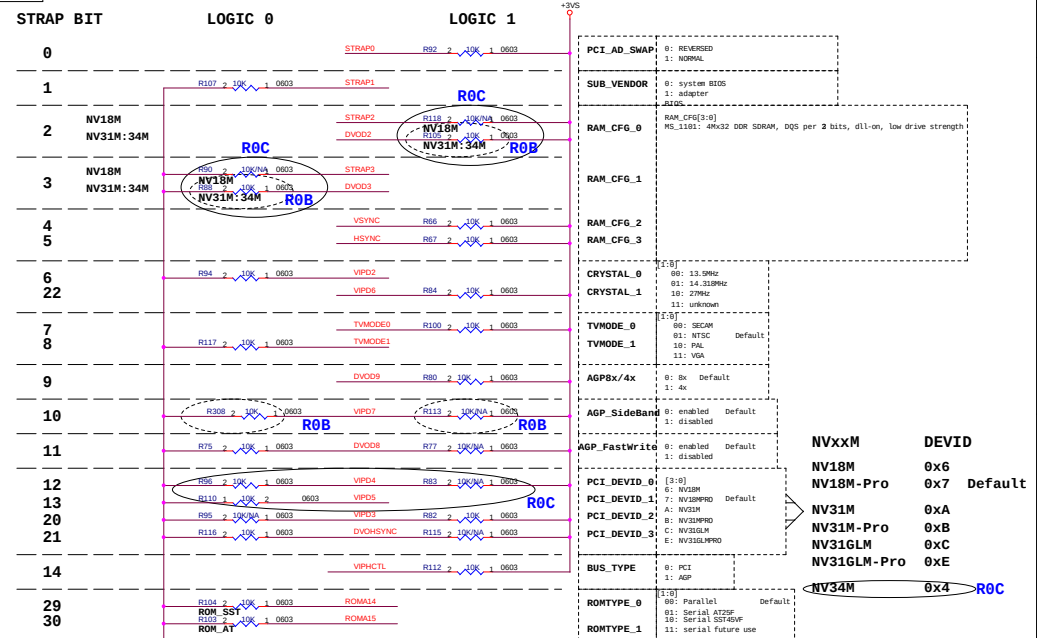
Layout Note:
W=12mil



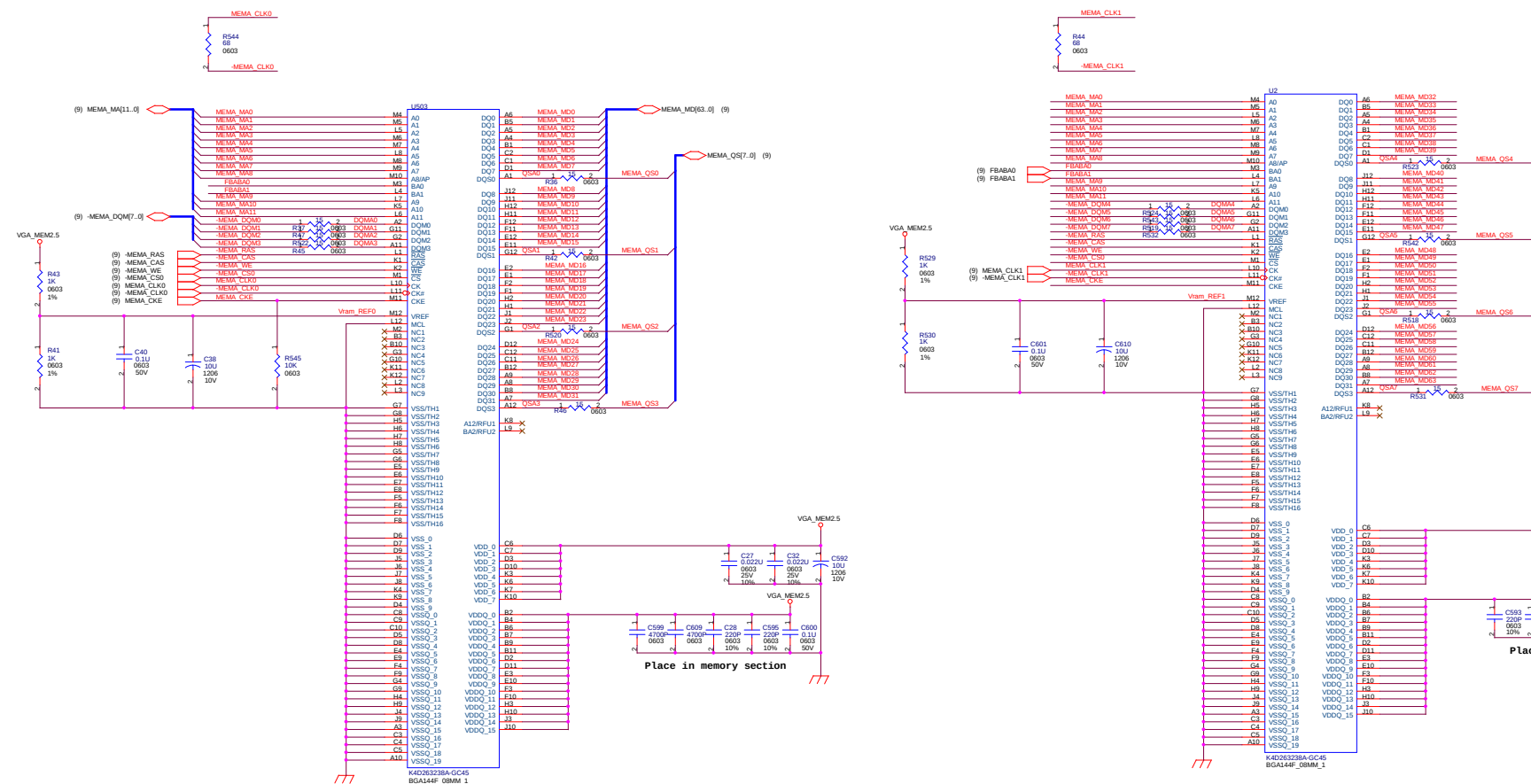
The diagram shows a microstrip layout for three GPIOs. The top two lines are labeled I2CCSCL and I2CCSDA. The bottom line is labeled GPIO8_THMCTL and is circled. A dimension line indicates a width of 12 mils for the bottom line.



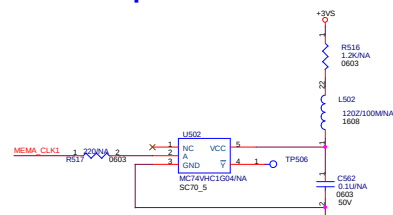
GPI0	DEFAULT STATE	USAGE
0	PD	Spread spectrum control
1	PD	Hot plug/unplug
2	PD	Panel backlight enable
3	PD	Panel power enable
4	PD	TBD
5	PD	Spread spectrum control
6	PU	HW suspend
7	PU	Dynamic NVDD voltage control
8	PU	Thermal monitor
9	PU	TBD



NV18M/NV31

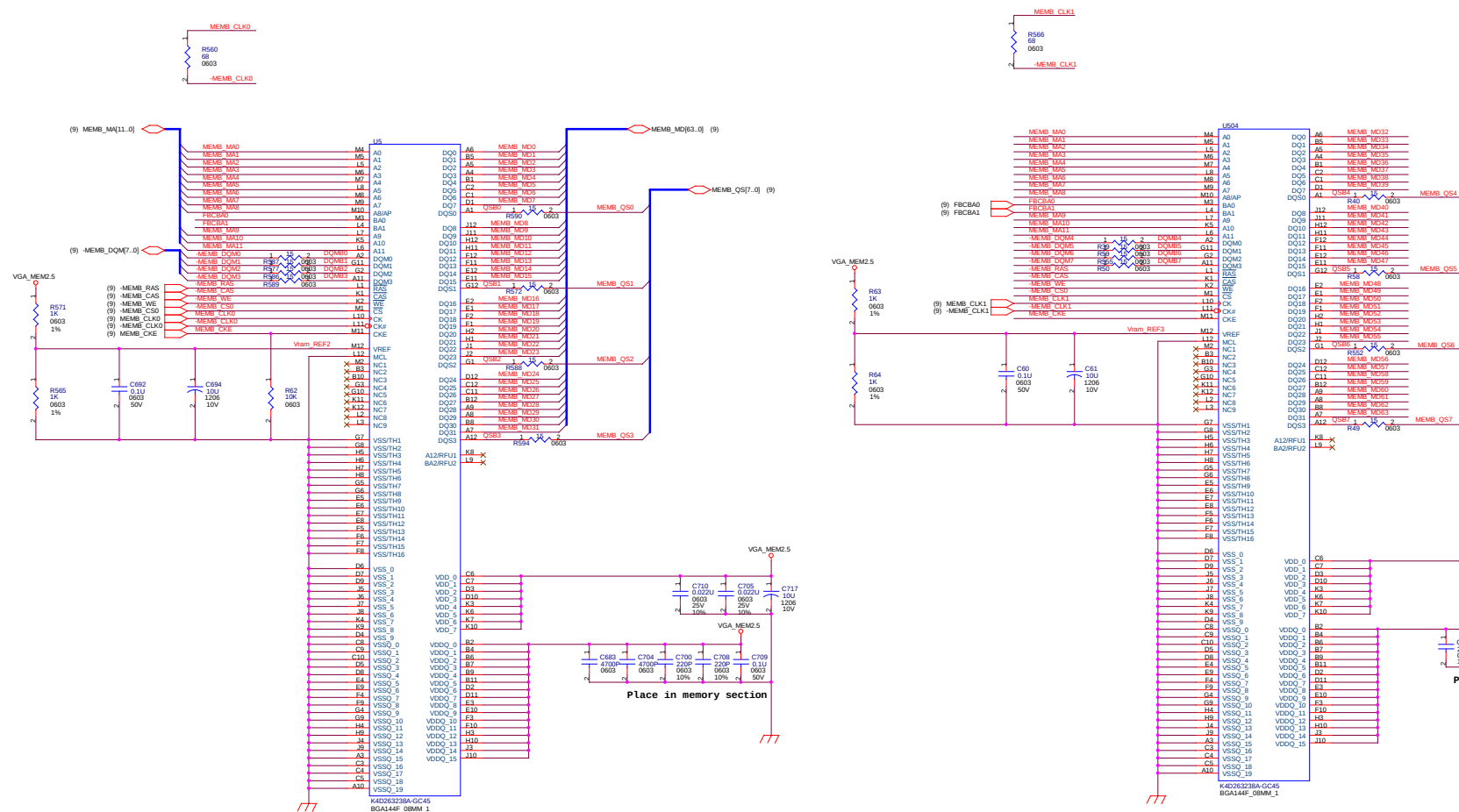


For EMI request



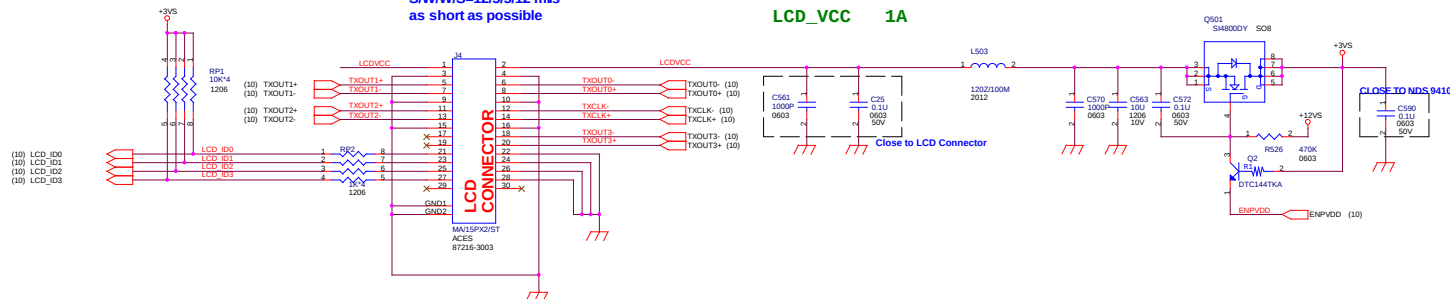
Title		NV34M(3)	
Size	Document	Rev	
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NV18M/NV31



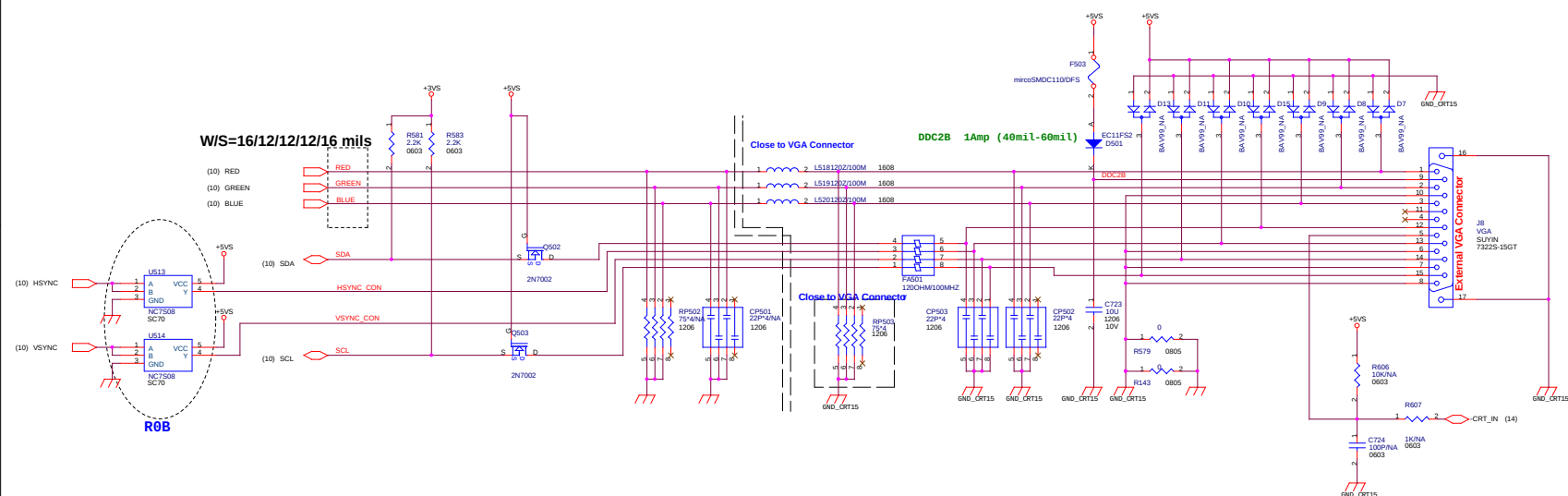
LCD & CRT INTERFACE

Layout Note: TXOUT0+1+2+3+0-1-2-3-
四組各自平行走線等長
SW/W/S=12/5/5/12 mils
as short as possible

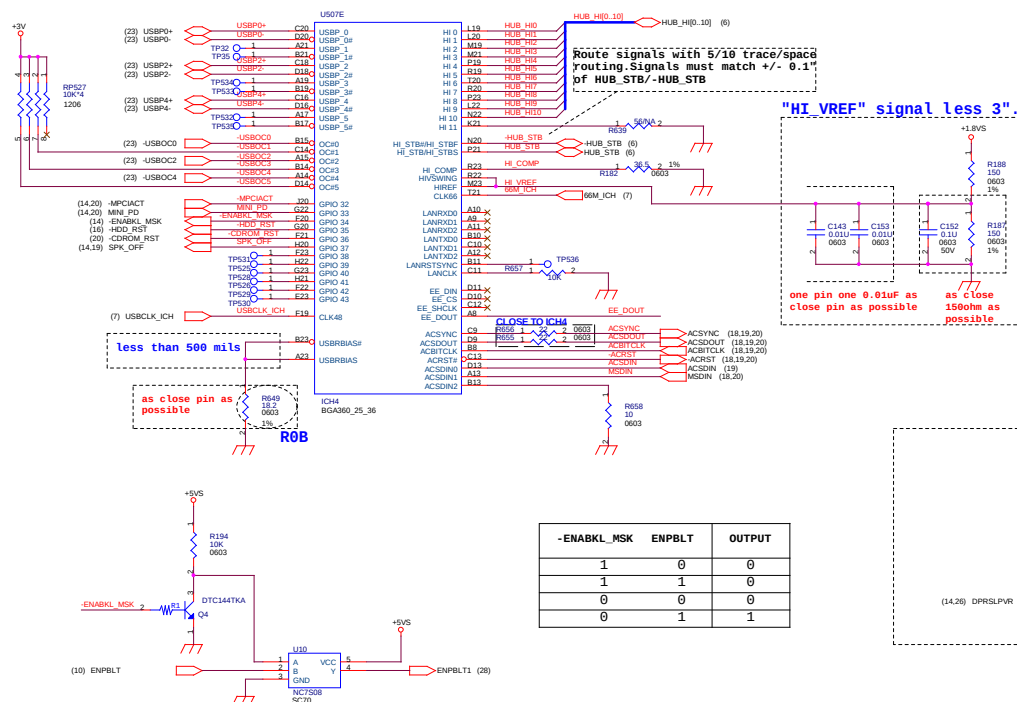


LCD ID Select Table

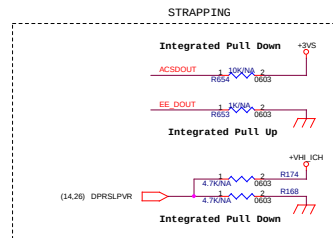
Display	LCD_ID3	LCD_ID2	LCD_ID1	LCD_ID0
LTN152W3 & B152EW01	0	0	0	1



I/O CONTROLLER HUB

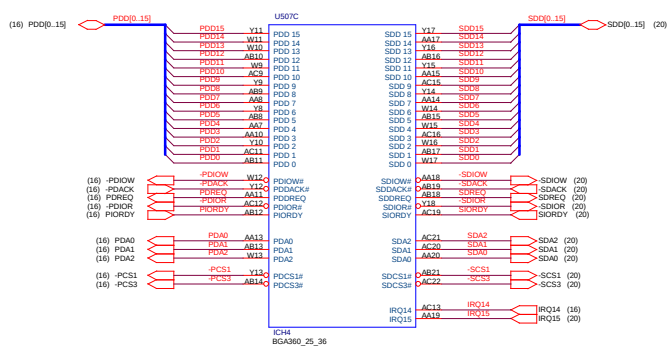


-ENABKL_MSK	ENPBLT	OUTPUT
1	0	0
1	1	0
0	0	0
0	1	1



STRAPPING AT RISING EDGE OF PWROK

STRAPPING PINS	FUNCTIONS
ACSDOUT	SAFE MODE
EEDOUT	RESERVED
-GNTA	OP-BLOCK SWAP OVERRIDE
DPRLSPVR	HUB INTERFACE TERMINATION SCHEME
HUB_TCH_COMP	HUB INTERFACE SCHEME(1.0 OR 1.5)
SBSPKR	NO REBOOT



GPIO CHARACTERISTIC LIST

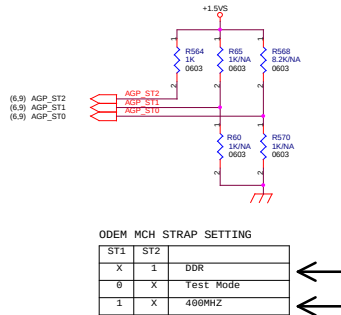
NAME	TYPE	POWER PLANE	CURRENT DEFINE
GPIO[0]	I	MAIN POWER WELL	-PCI_REQA
GPIO[1]	I	MAIN POWER WELL	-PCI_REQB
GPIO[2]	I	MAIN POWER WELL	-PCI_INTE
GPIO[3]	I	MAIN POWER WELL	-PCI_INTF
GPIO[4]	I	MAIN POWER WELL	-PCI_INTG
GPIO[5]	I	MAIN POWER WELL	-PCI_INTH
GPIO[6]	I	NOT Implemented	-AGP_BUSY
GPIO[7]	I	MAIN POWER WELL	X
GPIO[8]	I	RESUME POWER WELL	-SCI
GPIO[11]	I	RESUME POWER WELL	-SMBALERT
GPIO[12]	I	RESUME POWER WELL	-EXTSMI
GPIO[13]	I	RESUME POWER WELL	-CRT_IN
GPIO[16]	O	MAIN POWER WELL	X
GPIO[17]	O	MAIN POWER WELL	X
GPIO[18]	O	NOT Implemented	-STOP_PCI
GPIO[19]	O	NOT Implemented	-SUSA
GPIO[20]	O	NOT Implemented	-STOP_CPU
GPIO[21]	O	NOT Implemented	X
GPIO[22]	OD	NOT Implemented	-CPUPERF
GPIO[23]	O	NOT Implemented	X
GPIO[24]	I/O	NOT Implemented	-PCLKRUN
GPIO[25]	I/O	RESUME POWER WELL	SUSPEND
GPIO[27]	I/O	RESUME POWER WELL	-PCIRST_MSK
GPIO[28]	I/O	RESUME POWER WELL	PULL_HI
GPIO[32]	I/O	MAIN POWER WELL	-MPC1ACY
GPIO[33]	I/O	MAIN POWER WELL	MINI_PD
GPIO[34]	I/O	MAIN POWER WELL	-ENABKL_MSK
GPIO[35]	I/O	MAIN POWER WELL	-HDD_RST
GPIO[38]	I/O	MAIN POWER WELL	-CDROM_RST
GPIO[37]	I/O	MAIN POWER WELL	SPK_OFF
GPIO[38]	I/O	MAIN POWER WELL	X
GPIO[39]	I/O	MAIN POWER WELL	X
GPIO[40]	I/O	MAIN POWER WELL	X
GPIO[41]	I/O	MAIN POWER WELL	X
GPIO[42]	I/O	MAIN POWER WELL	X
GPIO[43]	I/O	MAIN POWER WELL	X



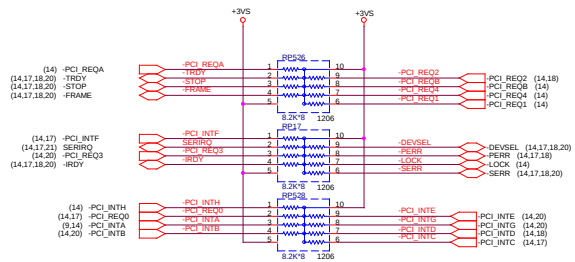
Title			
ICH4-M(2/2)			
Size	Document		Rev
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AGP BUS PULL UP/DOWN

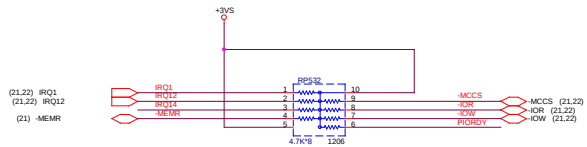
ST[1] has an internal pull-up straps on BPSB for 100Mhz



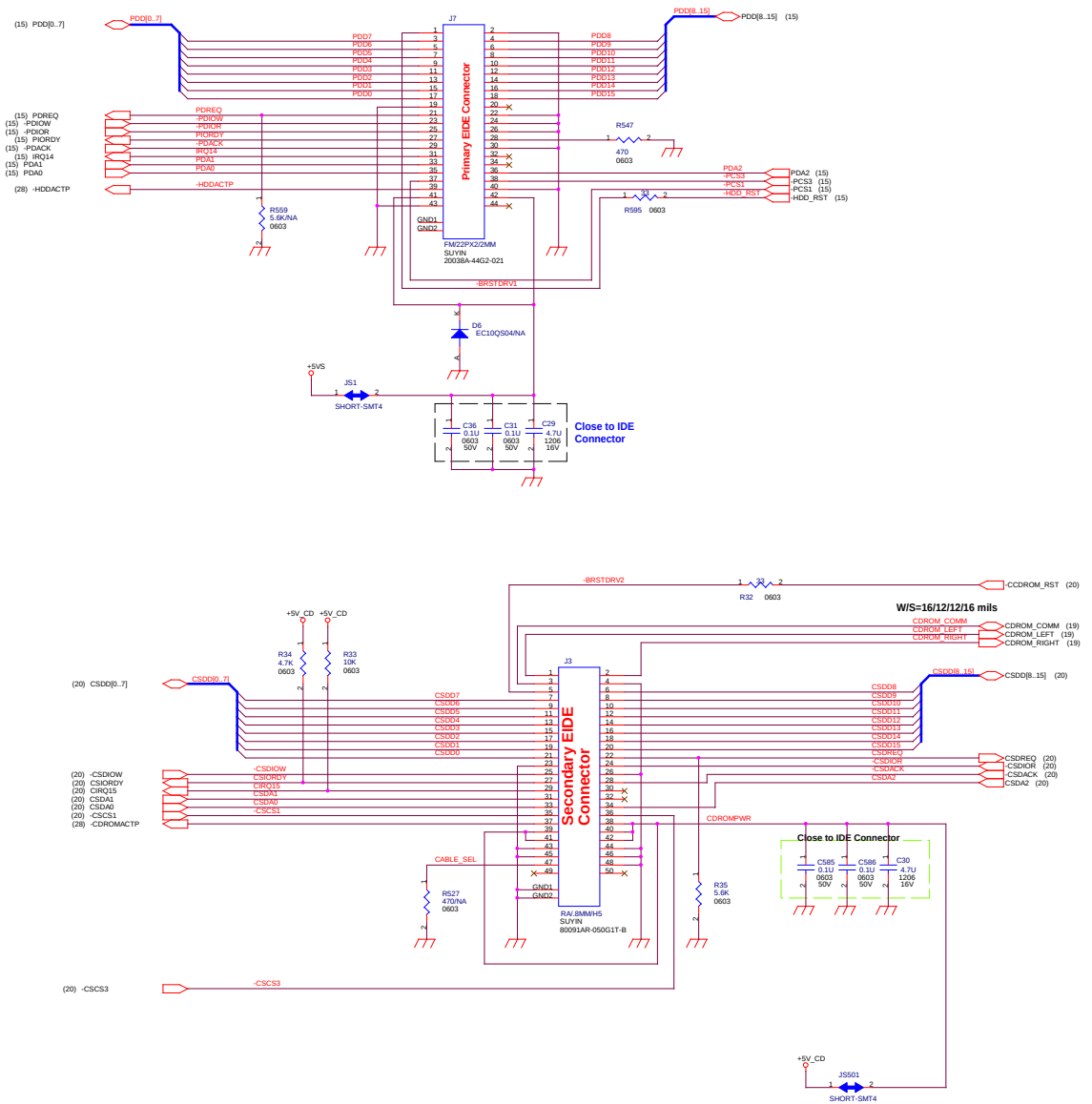
PCI BUS PULL UP/DOWN



ISA BUS PULL UP/DOWN

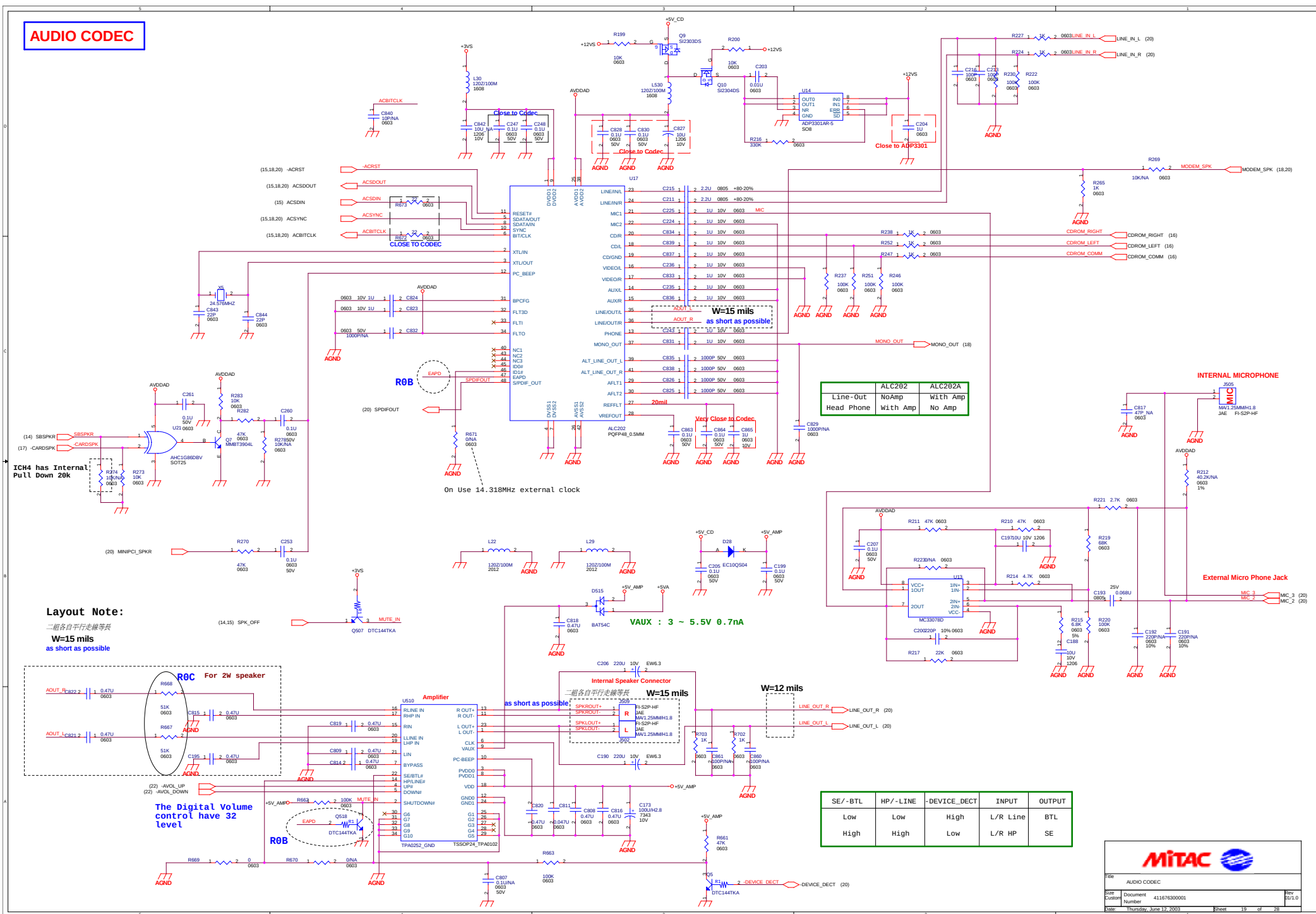


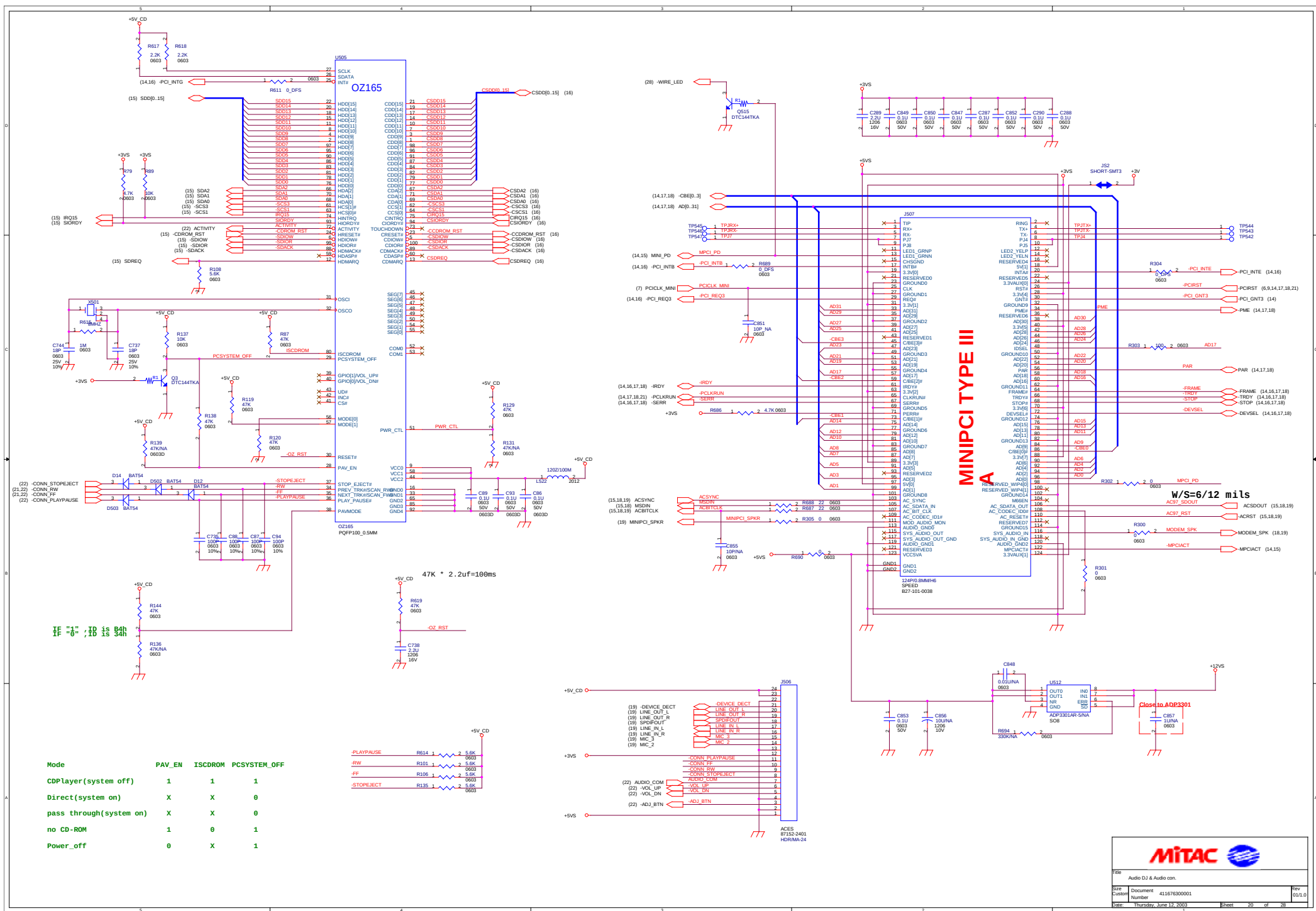
ENHANCED IDE



Title Enhance IDE			
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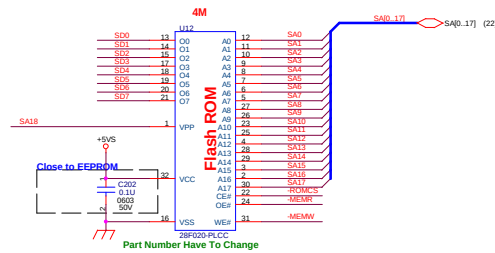
AUDIO CODEC



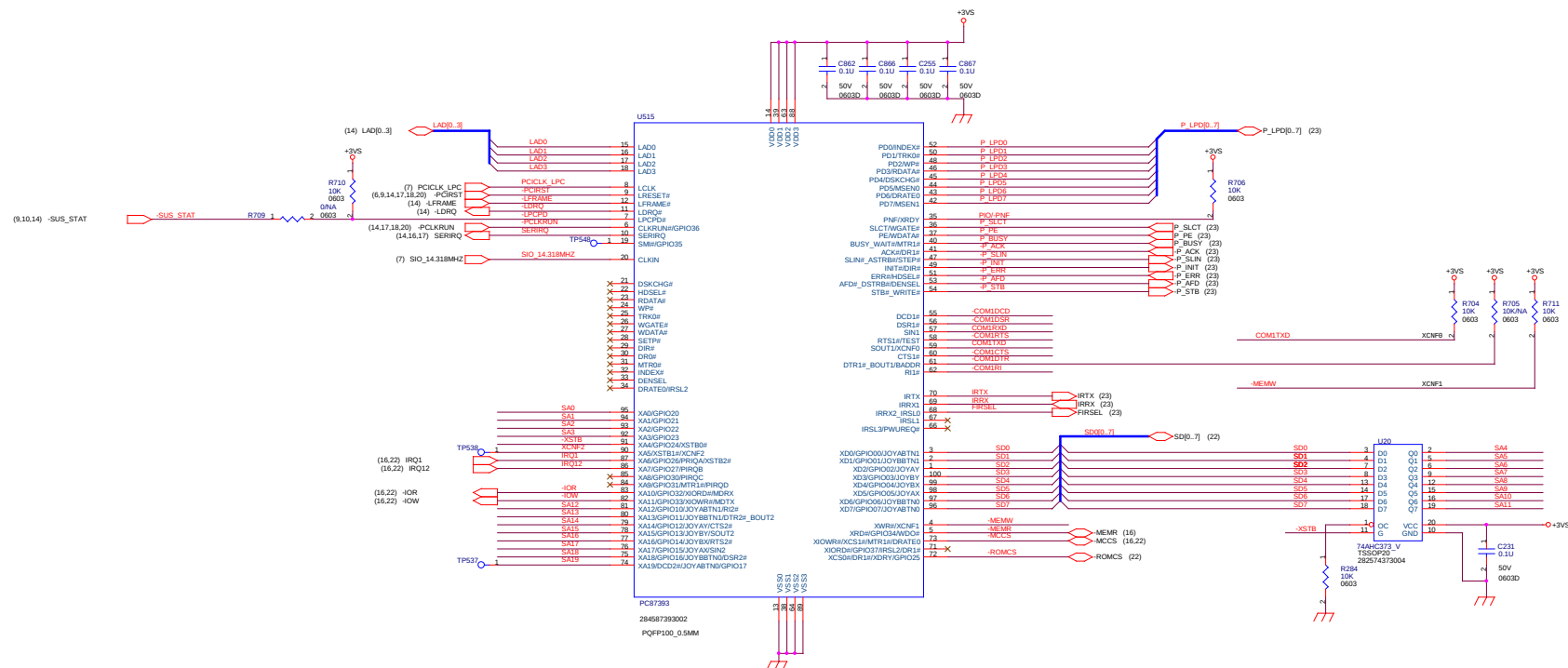
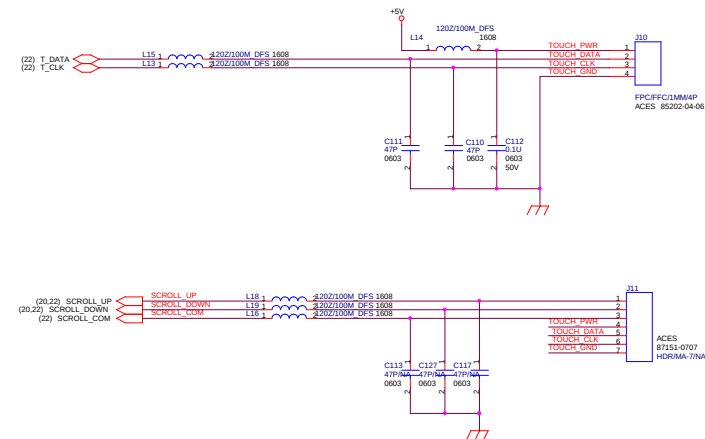


BIOS & T/P & SUPER I/O CHIP

BIOS ROM

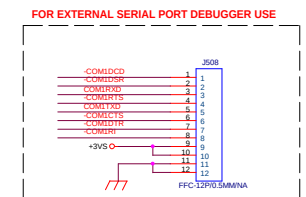


TOUCH_PAD

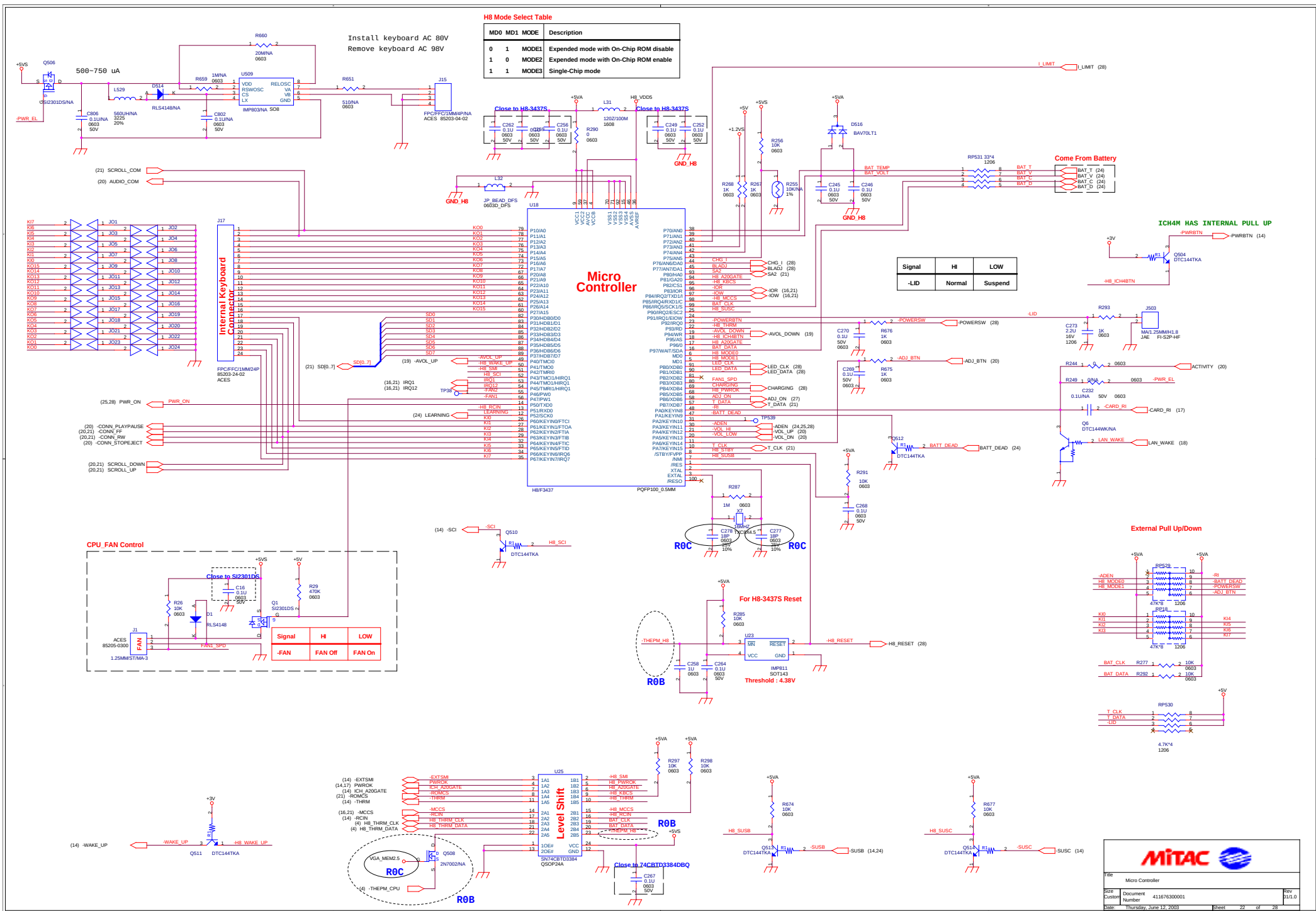


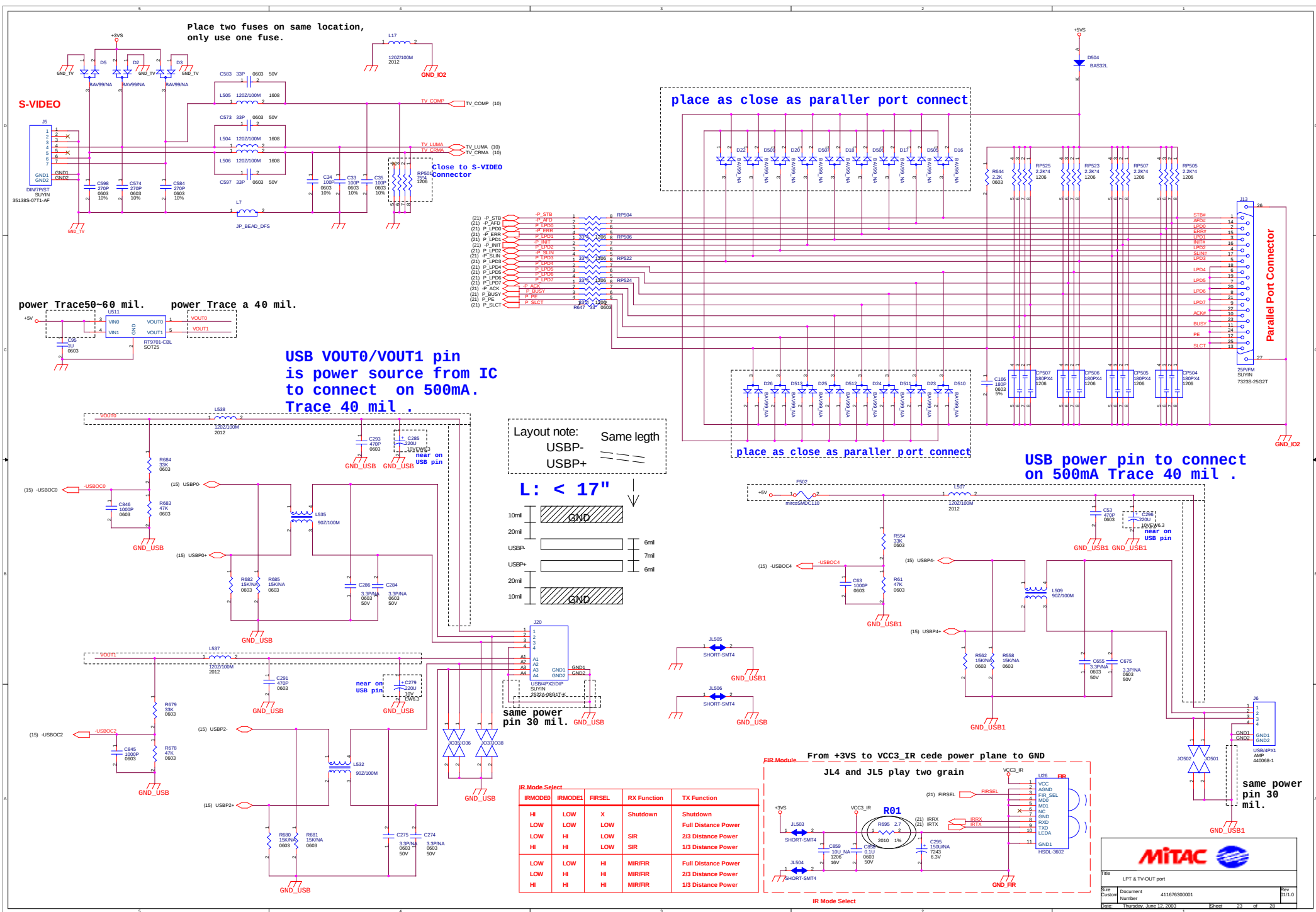
STRAP OPTION			
XCNF2	XCNF1	XCNF0	FUNCTIONALITY
X	0	0	NO BIOS
X	0	1	NORMAL MODE, XRDY DISABLE
0	1	0	LATCH MODE, XA12-19, XRDY ENABLE
1	1	0	LATCH MODE, GPIO 10-17, XRDY ENABLE
0	1	1	LATCH MODE, XA12-19, XRDY DISABLE
1	1	1	LATCH MODE, GPIO 10-17, XRDY DISABLE

BASE ADDRESS SELECT		
R643	INDEX REGISTER	DATA REGISTER
MOUNTED	4EH	4FH
OPEN	2EH	2FH

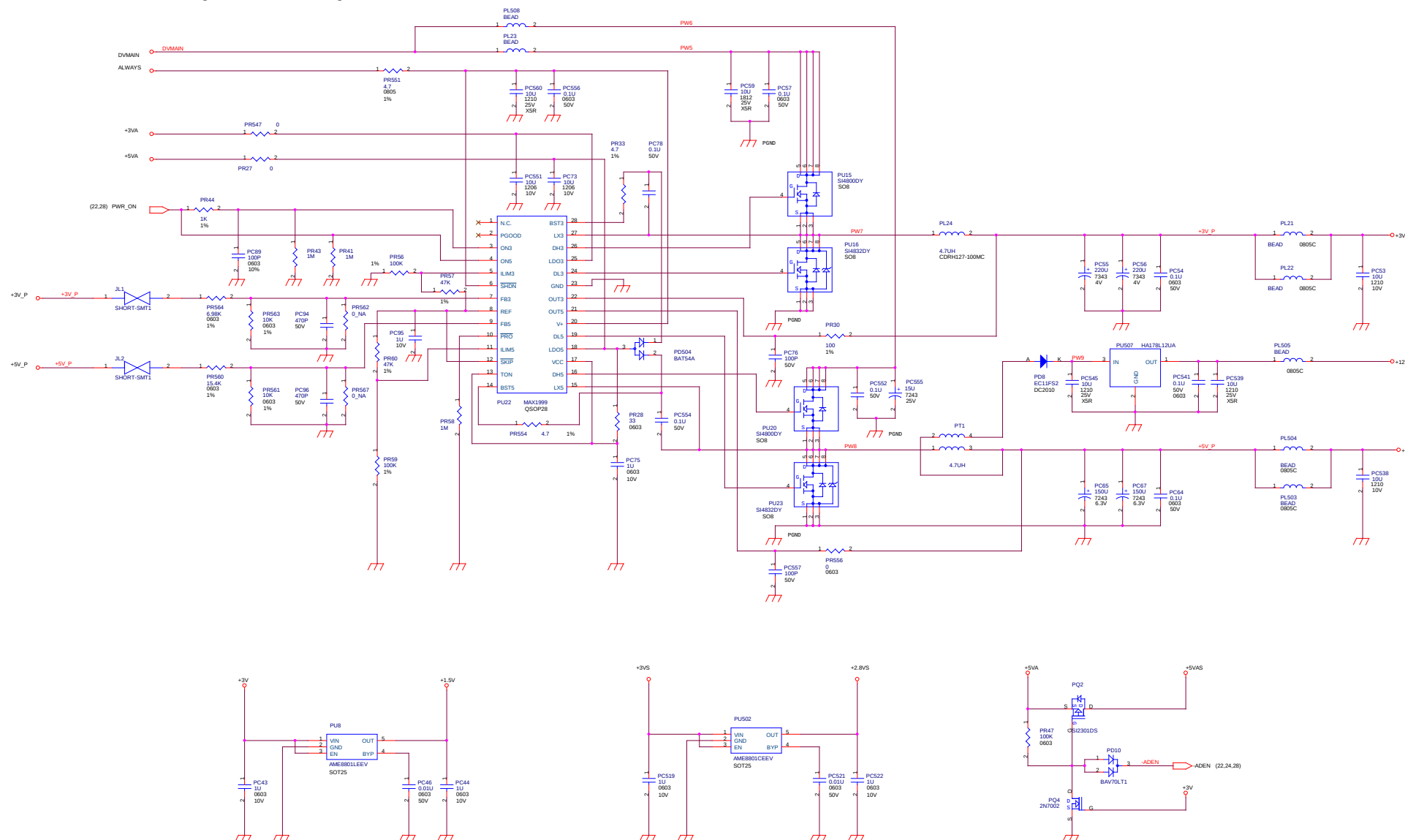


Title			
BIOS, SUPER-IO, TOUCHPAD			
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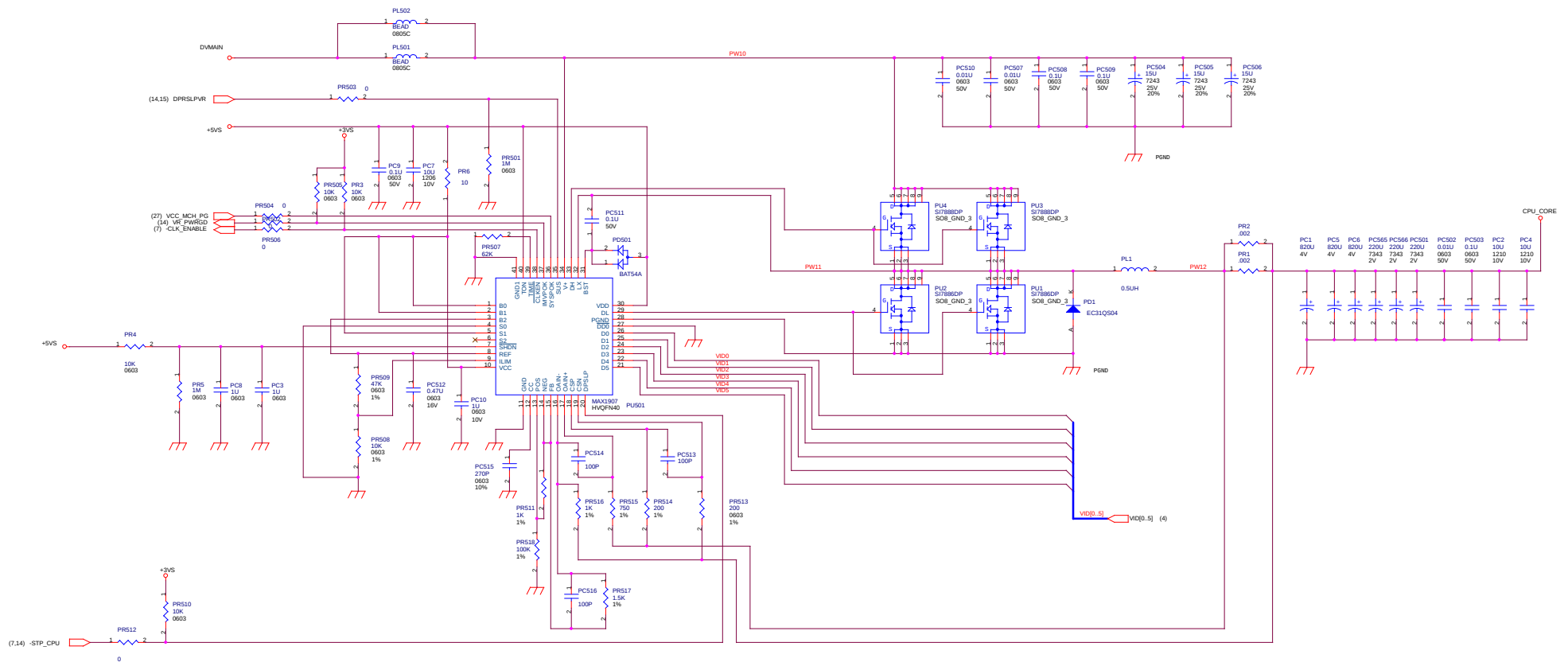




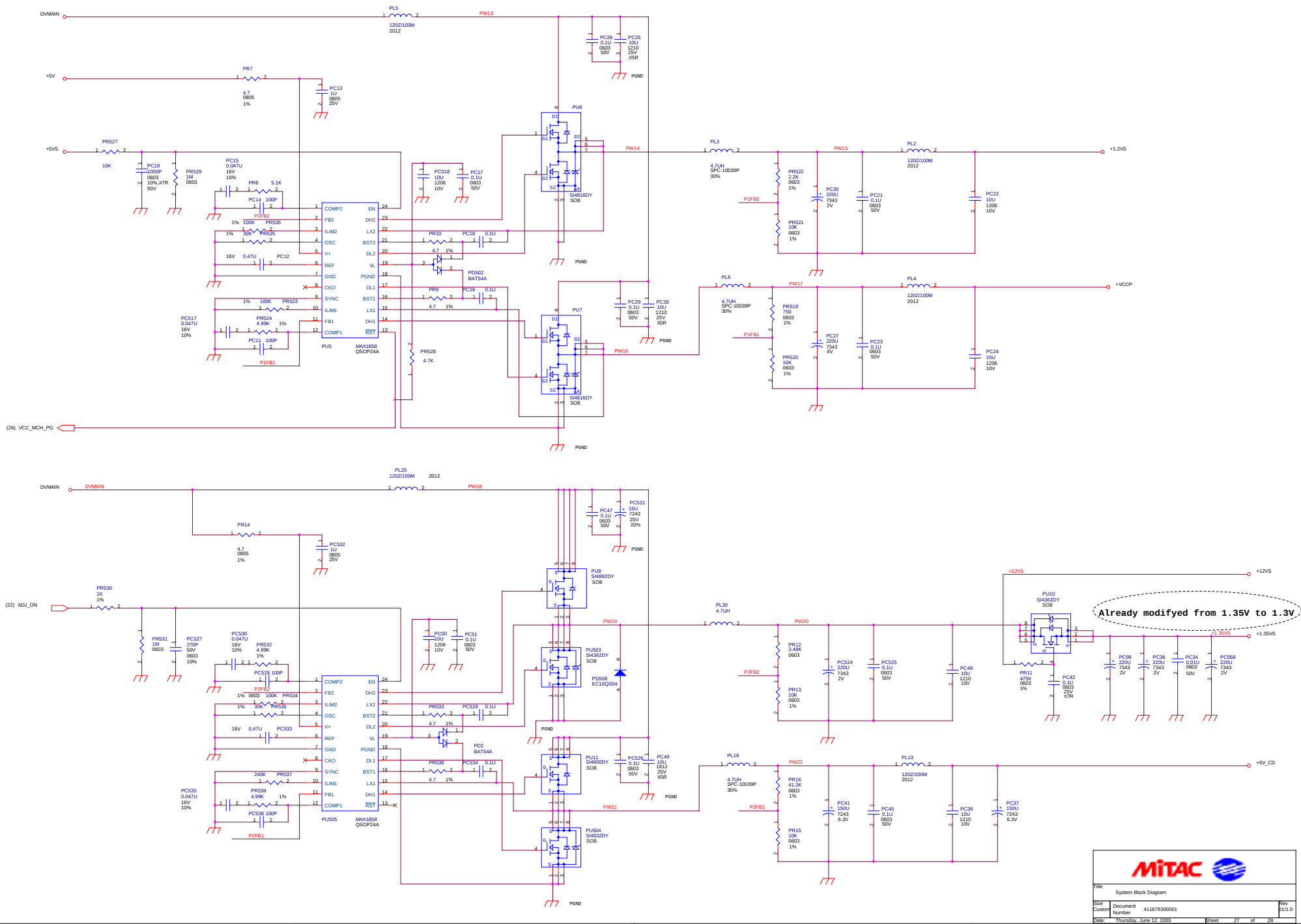
SYSTEM POWER (5V 3V 12V)

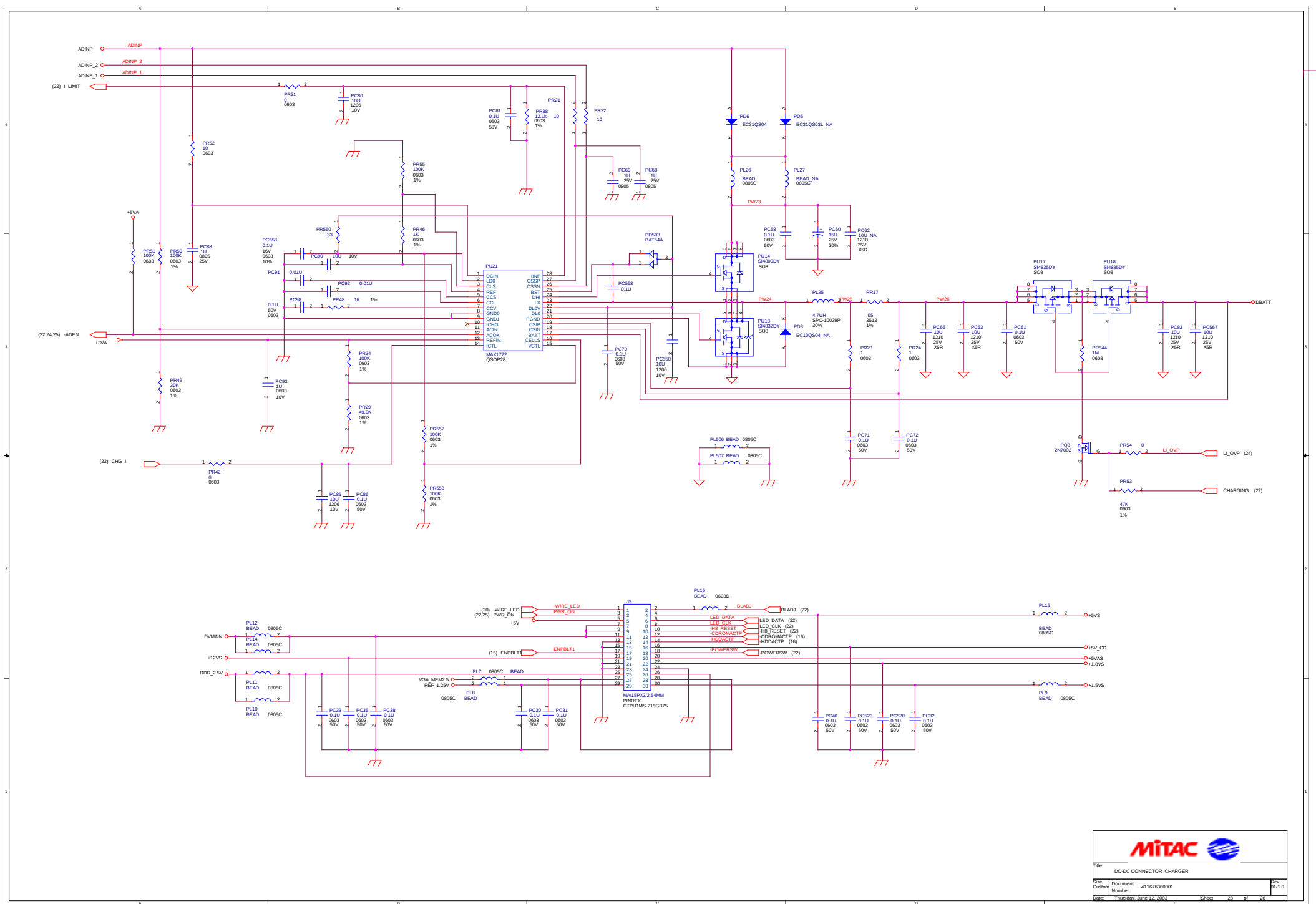


Title			
DC POWER			
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File	System Block Diagram
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AUDIO DJ BOARD

LINE_OUT_L/R Trace width/Space/Isolate must 15/15/15

Reference Material

- | | |
|---|-------------------------------|
| ❖ Intel Mobile Pentium M Processor | Intel, INC |
| ❖ Intel 82855 Memory Controller Hub (Odem) | Intel, INC |
| ❖ Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) | Intel, INC |
| ❖ 8060B Hardware Engineering Specification | <i>Technology Corp./MiTAC</i> |

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